

# Direct Conversion RF Digital Receiver in L-Band for QPSK

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## Abstract:

In today's world, radios exist in a multitude of items such as cell phones, computers, car door openers, vehicles, and televisions. Traditional hardware based radio devices limit cross-functionality and can only be modified through physical intervention. This results in higher production costs and minimal flexibility in supporting multiple waveform standards. By contrast, software defined radio technology provides an efficient and comparatively inexpensive solution to this problem, allowing multimode, multi-band and/or multi-functional wireless devices that can be enhanced using software upgrades. The processing on base band is carried out in MATLAB/ Simulink using QPSK Modulation. Necessary base band processing algorithms will be written in MATLAB/ Simulink to evaluate the performance of these algorithms. The direct conversion receiver is modeled and simulated using AD9361 with integration of Zed board and ADFMCOMMS2-EBZ board. Direct conversion receiver translates RF signal to base band signal in one stage. The model drastically reduces cost, design time, board size, weight power and results in high performance. It also reduces the problem of image frequency.

## Keywords

RF radio, QPSK, ASK, Modulation, Direct conversion Receiver, automatic gain control (AGC), etc.

## 1. Introduction

A number of definitions can be found to describe Software Defined Radio, also known as Software Radio or SDR. Software Defined Radio is defined as "Radio in which some or all of the physical layer functions are software defined". A radio is any kind

of device that wirelessly transmits or receives signals in the radio frequency (RF) part of the electromagnetic spectrum to facilitate the transfer of information. In today's world, radios exist in a multitude of items such as cell phones, computers, car door openers, vehicles, and televisions. Traditional hardware based radio devices limit cross-functionality and can only be modified through physical intervention. This results in higher production costs and minimal flexibility in supporting multiple waveform standards. By contrast, software defined radio technology provides an efficient and comparatively inexpensive solution to this problem, allowing multimode, multi-band and/or multi-functional wireless devices that can be enhanced using software upgrades.

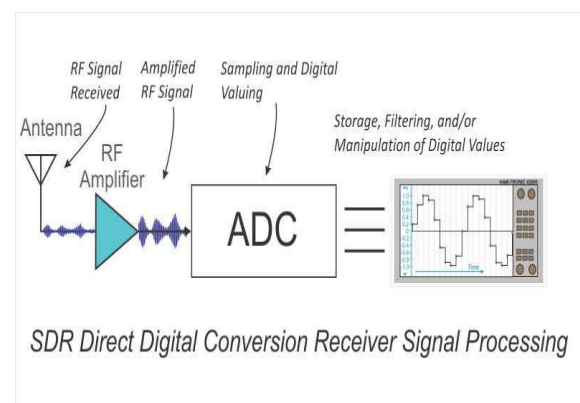
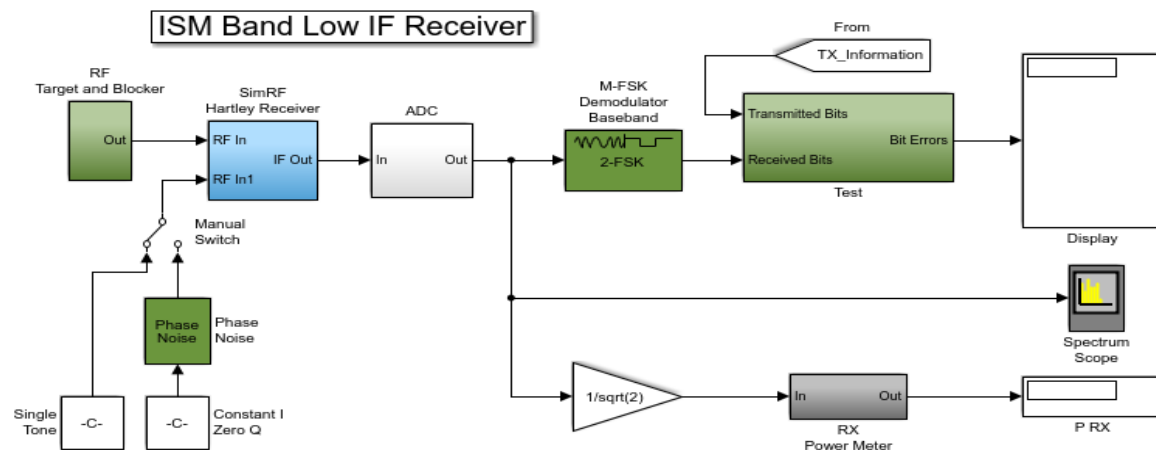


Fig 1: SDR Direct Digital Receiver

SDR defines a collection of hardware and software technologies where some or all of the radio operating functions (also referred to as physical layer processing) are implemented through modifiable software or firmware operating on programmable processing technologies.



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Fig 2: L-Band Direct Conversion Receiver

These devices include field programmable gate arrays (FPGA), digital signal processors (DSP), general purpose processors (GPP), programmable System on Chip (SoC) or other application specific programmable processors.

The use of these technologies allows new wireless features and capabilities to be added to existing radio systems without requiring new hardware.

The AD9361 is a high performance, highly integrated radio frequency (RF) Agile Transceiver designed for use in digital radio transceiver applications. Its programmability and wide band capability make it ideal for a broad range of transceiver applications. The device combines a RF front end with a flexible mixed-signal base band section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor. The AD9361 operates in the 70 MHz to 6.0 GHz range, covering most of the bands. Channel bandwidths from less than 200 kHz to 56 MHz are supported.

The ADFMCOMMS2-EBZ is a high speed analog module designed to show the AD9361, a high performance, a highly integrated RF agile transceiver used for RF applications such as 3G and 4G base station applications and software defined radios. Its programmability and wide band capability make it ideal for a broad range of transceiver applications. The device combines an RF front end with a flexible mixed-signal base band section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a

processor or FPGA. The AD9361 chip operates in the 70MHz to 6GHz range, covering most licensed and unlicensed bands. The boards, due to discrete external components may have less performance on some of the RF input/output connectors. The AD9361 supports channel bandwidths from less than 200 kHz to 56MHz by both changing sample rate, and by changing digital filters, and decimation inside the device itself.

ZED Board is an Evaluation and Development Board based on the Xilinx TM-7000 All Programmable System on Chip (AP SoC). It is a combination of dual Cortex-A9 processing system (PS) with 85000 series 7 programmable logic (PL) cells. The zynq-7000 AP SoC can be targeted for use in many applications. The ZED board's robust mix of on board peripherals and expansion capabilities make it ideal platform for both novice and experienced designers.

## 2. Direct Conversion Architecture

A direct conversion receiver is also known as synchrodyne, homodyne, or zero-IF receiver. Direct conversion receiver demodulates the incoming radio signal using synchronous detection, driven by a local oscillator whose frequency is same as, or very close to the carrier frequency of the incoming signal. This is in contrast to the standard super heterodyne receiver where this is accomplished only after an initial conversion to an intermediate frequency. The simplification of performing only a single frequency conversion reduces the complexity of the circuit.

### A. Operation Principle of Direct conversion Receiver

A direct conversion receiver converts the modulated signal to the baseband signal using a single frequency conversion. It avoids the complexity of the two or more stages of frequency conversions, IF stage, image rejection issues of super heterodyne receiver structure. The received radio signal frequency is directly fed into the frequency mixer, same as in super heterodyne receiver but the frequency of the local oscillator is identical to that of the incoming radio signal frequency. The output is a demodulated signal just as would be obtained from a super heterodyne receiver using synchronous detection following an intermediate frequency stage.

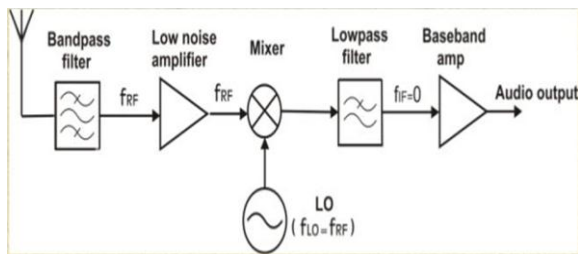


Fig 3: Direct Conversion Receiver.

### B. Technical issues

To match the performance of the direct conversion receiver with that of super heterodyne receiver a number of functions normally addressed by the IF stage must be accomplished at the baseband. Since there is no high gain IF amplifier utilizing automatic gain control (AGC), the baseband output level may vary over a wide range dependent on the received signal strength. This is one major challenge which limited the practicability of the design. Another issue is the inability of this design to implement envelop detection of AM signals. Thus direct demodulation of AM or FM signals requires the phase locking the local oscillator to the carrier frequency, a much more demanding task compared to the more robust envelop detector or ratio detector at the output of an IF stage in a super heterodyne design. This can be avoided in direct conversion design using quadrature detection followed by digital signal processing. Using software radio techniques, the two quadrature outputs can be processed in order to perform any sort of demodulation and filtering on down converted signals from frequencies close to the local oscillator frequency.

### C. Advantages

1. Lower complexity and power consumption since there are no IF amplifiers, IF bandpass filters, IF local oscillators, which has the ability to reach the 'one chip goal'.
2. No image frequency.

### D. Disadvantages

The local oscillator signal leaking to the antenna because of poor reverse isolation through the mixer and RF amplifier, a large near channel interferer leaking into the local oscillator port of the mixer.

The receiver is a **direct conversion system** that contains a low noise amplifier (LNA), followed by matched in-phase (I) and quadrature (Q) amplifiers, mixers, and band shaping filters that down convert received signals to baseband for the purpose of digitization. External LNAs can also be interfaced to the device, allowing designers the flexibility to customise the receiver front end for their specific application.

Gain control is achieved by following a pre-programmed gain index map that distributes the gain among the blocks for optimal performance at each level. This can be achieved by enabling the internal AGC in either fast or slow mode or by using manual gain control, allowing the BBP to make the gain adjustments as needed. Additionally, each channel contains independent RSSI measurement capability, dc offset tracking, and all circuitry necessary for self-calibration.

The receivers include 12-bit, sigma-delta ADCs and adjustable sample rates that produce data streams from the received signals. The digitized signals can be conditioned further by a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate.

## 3. Design Methodology

### A. QPSK Transmitter And Receiver Using AD9361

The ADFMCOMMS2-EBZ is a very high speed analog module. It is designed to show the AD9361, a high performance and highly integrated RF agile transceiver used for RF applications. The RF

applications include 3G and 4G base station applications and Software Defined Radios. The programmability and wide band capability make it ideal for broad range of transceiver applications. The device combines RF front end with a base band section and integrated frequency synthesizers, simplifying design-in by providing a digital interface to FPGA or a processor.

The ADFMCOMMS2-EBZ can be user configured for optimum performance in the 2.4 - 2.5 GHz band. In this configuration it may exhibit diminished RF performance on tuned frequencies or programmed configurations, outside of this band. This configuration is primarily intended to provide RF engineers with the ability to connect the AD9361 to an RF test bench which include Vector Signal Analyzer, Signal generator and achieve its optimum performance.

**a) QPSK Transmitter using AD9361**

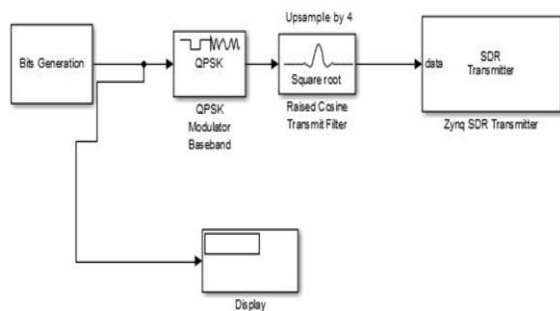


Fig 4: QPSK transmitter using AD 9361

The system performs four major processes. They are

1. Bit generation
2. Baseband modulation
3. Pulse shaping and up sampling
4. Sending baseband data to SDR hardware

**1. Bit Generation**

The Bit generation subsystem uses a MATLAB workspace variable as the payload of a frame. Each frame consists of 200 bits. The first 26 bits represents the header of a frame which are produced by the 13 bit barker code. The 26 header bits results in 13 symbol barker code which is used as a preamble. The preamble is used to overcome the channel impairments in the receiver. The first 105 bits of payload are ASCII representation of Hello world

000, Hello world 001....., and Hello world 099. The remaining 69 bits of payload are random bits. The payload bits are scrambled to guarantee a balanced distribution of zeros and ones for the timing recovery operation which is present in the receiver.

**2. Baseband modulation**

The output of the bits generation subsystem is given to the QPSK Modulator Baseband block. It modulates pairs of bits from the output of bit generation subsystem to QPSK constellation points using gray mapping. Each QPSK symbol is represented by one complex sample.

**3. Pulse Shaping and Upsampling**

The output of the QPSK Modulator block is given to the Raised Cosine Transmit Filter block. It performs root raised cosine pulse shaping with a roll off factor of 0.5. This block also upsamples the baseband signal by a factor of 4.

**4. Sending Baseband data to SDR Hardware**

The ZED Board and AD FMCOMMS2 Transmitter block sends baseband data to the SDR hardware over ethernet. The FPGA sends the baseband data to match the AD9361 baseband sample rate, AD9361 also upsamples the signal to RF and transmits it over the air. The rate at which the model runs is determined by the Baseband sample rate in Zynq SDR Transmitter block, not by the simulation sample time.

**b) QPSK Receiver using AD9361**

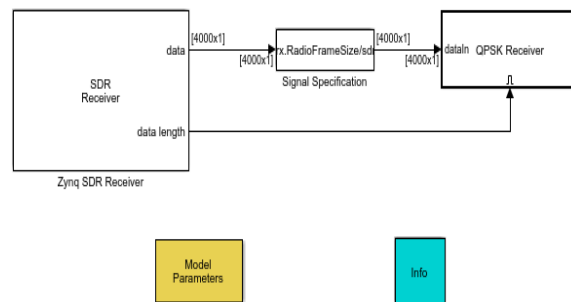


Fig 5: QPSK Receiver using AD 9361

The ZED Board and FMCOMMS2 Receiver block receives the data from the ZED Board and FMCOMMS2 Transmitter block over Ethernet. The SDR Receiver block sends the data received from the transmitter to the signal specification block. The

signal specification block is used to impart a sample rate on the receiver block data output.

The system performs the following operations. Automatic Gain Control, Raised Cosine Receive, Filter Coarse Frequency Compensation, Fine Frequency Compensation, Timing Recovery, Data Decoding.

### 1. Automatic Gain Control

The phase error detector gain of the phase and timing error detectors is proportional to the received signal amplitude and the average symbol energy. The inputs at the carrier recovery and timing recovery loops must be stable to ensure an optimum loop design.

The AGC's output value is 1/upsampling factor. In this case the upsampling factor is set to 4 so the AGC sets its output power to 0.25. So the equivalent gains of the phase and timing error detectors remain constant over time. The AGC is placed before the Raised Cosine Receive filter so that the signal amplitude can be measured with an over sampling factor of 4, thus improving the accuracy of the estimate. The AGC subsystem updates its gain after each block of 10 QPSK symbols in order to smooth out variations in signal amplitude.

### 2. Raised Cosine Receive Filter

The Raised Cosine Filter provides matched filtering for the transmitted wave. It also downsamples the input signal by a factor of 2 and with a Roll - off factor of 0.5

### 3. Coarse Frequency Compensation

The coarse frequency compensation subsystem corrects the input signal with a rough estimate of the frequency offset. The coarse frequency compensation subsystem is shown in the figure below. This subsystem contains the Find frequency offset subsystem. It uses a baseband QPSK signal with a phase index 'n', frequency offset  $\Delta f$  and phase offset  $\Delta\Phi$  expressed as  $e^{j(\frac{n\pi}{2} + \Delta f t + \Delta\Phi)}$ ,  $n = 0,1,2,3$ . First the subsystem raises the input signal to the power of 4 to obtain  $e^{j(4ft + 4\Delta\Phi)}$ , which is not done by the QPSK modulation. Then it performs an FFT on the modulation independent signal to estimate the tone at 4 times the frequency offset.

After dividing the estimate by 4, the phase/frequency offset block corrects the frequency offset. Residual frequency offset is present even after the coarse frequency compensation. Residual frequency results in the slow rotation of the constellation. The Fine Frequency Compensation subsystem is used to compensate residual frequency.

The FFT size and Number of Spectral Averages for the coarse frequency subsystem can be tuned to see the effect of estimation accuracy and the tolerance to a high noise level. The resolution of the estimate is the frequency spacing between two adjacent FFT points. Larger FFT size is required to get more accurate frequency estimate but large FFT size increases the computation burden. If the resolution of the coarse frequency compensation subsystem is low, then fine frequency compensation subsystem must have a wider frequency tracking range.

The FFT output may have some outliers in the estimation results because of the existence of the noise and zero padding of the input. To overcome this the Number of spectrum averages can be adjusted to average the FFT result across multiple frames. The larger number of spectrum Averages improves the robustness of the coarse frequency estimation, but it also increases the computational burden. Also, the fourth power operation can correctly estimate an offset only if the offset satisfies the following inequality:

$$4 * \Delta f_{max} \leq f_s/2, \text{ or}$$

$$4 * \Delta f_{max} \leq 2 * R_{sym}/2, \text{ or}$$

$$\Delta f_{max} \leq R_{sym}/4.$$

### 4. Fine Frequency compensation

The fine frequency compensation subsystem implements a phase locked loop to track the residual frequency offset and phase offset in the input signal. The PLL uses a Direct Digital Synthesizer to generate the compensating phase that offsets the residual frequency and phase offsets. The phase offset estimate from DDS is the integral of the phase error output of the loop filter.

The Phase Error Detector (PED) generates the phase error. A proportional plus integral Loop filter, filters the error signal and gives it to the DDS. The

loop bandwidth and the Loop damping factor are tunable for the loop filter. The default normalized loop bandwidth is 0.06 and default damping factor is 2.5 (over damping) so that the PLL quickly locks to the intended phase while introducing minimal phase noise.

### 5. *Timing Recovery*

The Timing Recovery subsystem implements a PLL, to correct the timing error in the received signal. The input of the timing recovery subsystem is oversampled by 2. The Timing Recovery subsystem generates one output sample for every two input samples. The NCO Control is to generate the control signal for the Modified Buffer that selects the interpolants of the interpolation filter. This control signal also enables the timing error detector (TED), so that it calculates the timing errors at the correct timing instants. The NCO Control Subsystem updates the timing difference for the interpolation filter, generating interpolants at optimum sampling instants. The interpolation filter is a Farrow parabolic filter with  $\alpha = 0.5$ . The filter uses an  $\alpha$  of 0.5 so that all the filter coefficients become only 1, -1/2 and 3/2 which simplifies the structure of the interpolator. Based on the interpolants, timing errors are generated by a zero crossing Timing Error Detector, filtered by a tunable proportional plus integral Loop Filter and fed into the NCO Control for a timing difference update. The loop bandwidth and loop damping factor are tunable for the loop filter. The default normalized loop bandwidth is set to 0.01 and the default damping factor is set to unity (critical damping) so that the PLL quickly locks to the correct timing while introducing little phase noise.

When the timing error reaches symbol boundaries, there will be one extra or missing interpolant in the output. The TED implements bit stuffing or bit skipping to handle the extra or missing interpolants.

The timing recovery loop normally generates 100 QPSK symbols per frame, the one output symbol for every two input samples. It also runs the timing strobe which runs at input sampling rate. The strobe value is a sequence of alternating ones and zeroes. This occurs when the relative delay between Tx and Rx contains some fractional part of one symbol period and the integer part of the delay (in symbols) remains constant. If the integer part of the relative

delay changes, the strobe value can be two consecutive zeros or two consecutive ones. Then the timing recovery loop generates 99 or 101 QPSK output symbols per frame. The downstream processing must use a frame size of 100 symbols, which is ensured by the Modified Buffer subsystem.

The Modified Buffer subsystem uses the strobe to fill up a delay line with properly sampled QPSK symbols. As each QPSK symbol is added to the delay line, a counter increments the number of symbols in the line. At each sampling instant, the delay line outputs a frame of size 100 to the Data Decoding subsystem. The Data Decoding subsystem runs on its received data only when its enable signal goes high, i.e. each time exactly 100 valid QPSK symbols are present at the Modified Buffer.

The Timing Recovery subsystem relies on a stable constellation which does not rotate over time. This requires an accurate frequency offset compensation. If the actual frequency offset exceeds the maximum frequency offset that can be tracked by the coarse frequency compensation subsystem. The tracking range can be increased by increasing the oversampling factor. Another way to adjust the tracking range is to implement a rotationally-invariant timing error detector first and correct the rotation afterwards.

### 6. *Data Decoding*

The Data Decoding subsystem performs frame synchronization, phase ambiguity resolution, demodulation and text message decoding. The subsystem uses a QPSK-modulated Barker code, generated by the Bits Generation subsystem, to correlate against the received QPSK symbols and achieve frame synchronization. The Compute Delay subsystem correlates the data input with the QPSK modulated Barker Code, and uses the index of the peak amplitude to find the delay.

The carrier phase PLL of the Fine Frequency Compensation subsystem may lock to the unmodulated carrier with a phase shift of 0, 90, 180, or 270 degrees, which can cause a phase ambiguity. The Phase offset Estimator subsystem determines this phase shift. The Phase Ambiguity Correction and Demodulation subsystem rotates the input signal by the estimated phase offset and demodulates the corrected data. The payload bits are descrambled, and the first 105 payload bits are extracted and stored

in a workspace variable. All the stored bits are converted to characters and printed out at the MATLAB command window while the simulation is running.

**B. Hardware Generation Model**

In order to generate HDL code for QPSK Transmitter and Receiver a hardware generation model is developed in the simulink and the performance of the model is verified. Then HDL IP core is generated using HDL workflow advisor and the bit stream is

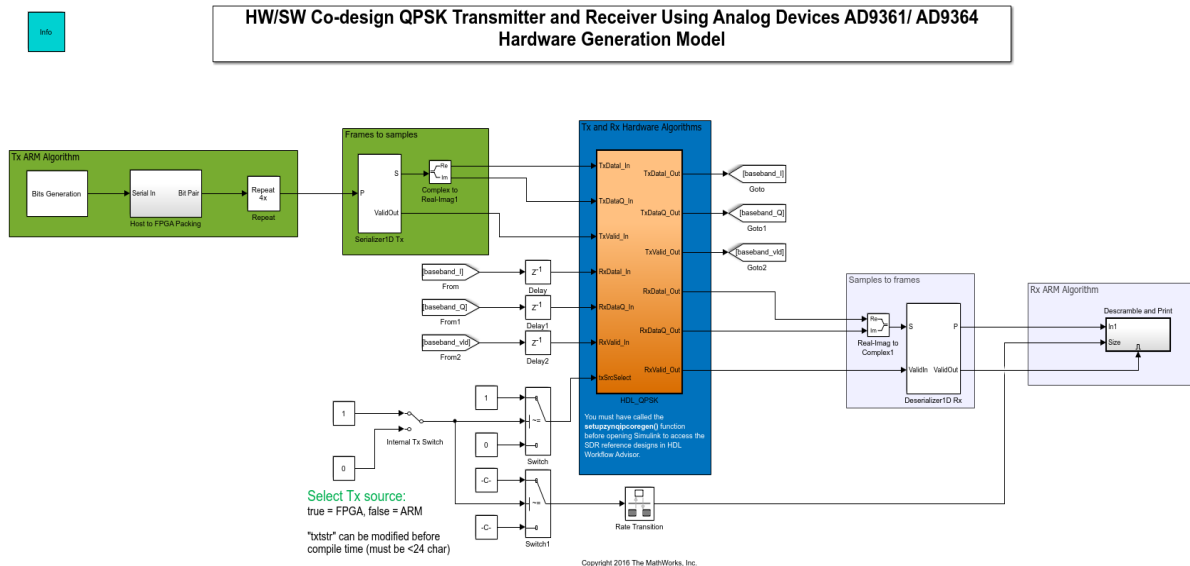


Fig 6: Hardware generation model

generated. The generated bit stream is deployed on the Zynq board and the performance of the system is verified.

**4. Results and Discussion**

AD 9361 is connected through the FMC present on the ZED Board. The ZED Board will transmit and receive the data through the Ethernet port from Simulink and AD9361. The SDR block in the

Simulink model will send the message to the ZED Board through the Ethernet cable. The ZED Board will send the transmitted message to the transmitter of AD9361, which will up convert the received signal and is given to the receiver port of AD9361 through the loop back cable. It will down convert the received signal and the demodulation of the signal is done in the Simulink model.

**A. Spectrum of Transmitted data**

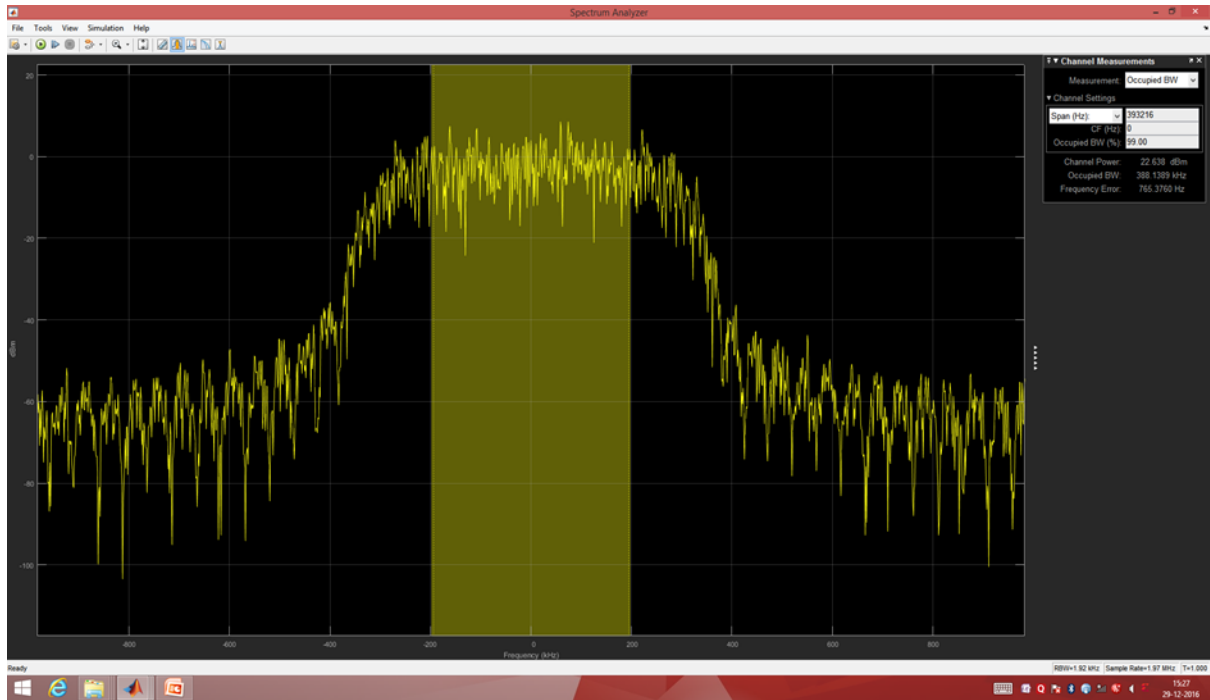


Fig 7: Transmitted spectrum when  $\alpha = 0.5$

**B. Spectrum of Received data**

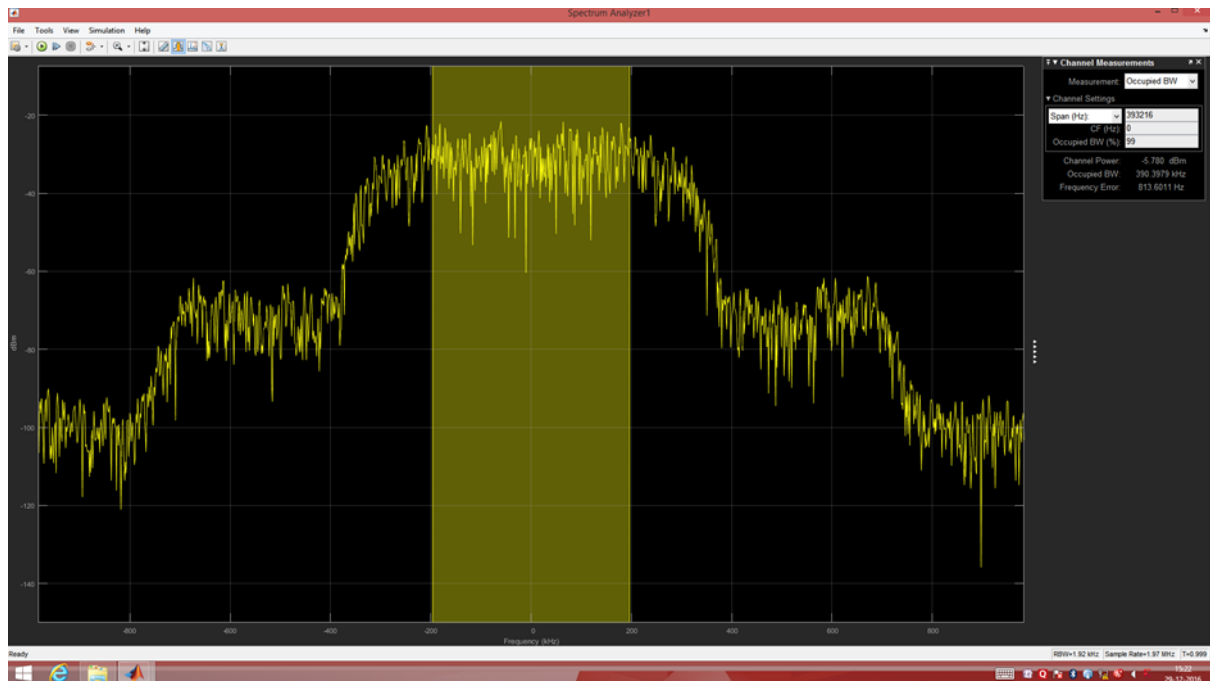


Fig 8: Received Spectrum when  $\alpha = 0.5$

If Roll of factor of Raised Cosine Filter is  $\alpha=0.5$

Theoretically,

$$\text{Bandwidth} = (1 + \alpha) * \text{symbol Rate}$$



$$= (1+0.5)*260\text{KHZ}$$

$$= 390\text{KHZ}$$

Practically,

$$\text{Bandwidth} = 388.1389\text{KHZ.}$$

**C. Comparison of Bandwidths**

Roll off factor $\alpha$	Bandwidth in KHZ(Theoretically)	Bandwidth in KHZ(Practically)
0.5	390	388.1389
0.6	416	406.8734

The symbol rate is set to 260KHZ and the sampling frequency is set to 520841, it can be upto 6MHZ. The centre frequency is set to 1.21GHZ which is in the L-band frequency range. The L-Band ranges from 960 – 1240 KHZ. The spectrum analyser output is as shown in the figure below which also has the centre frequency of 1.21GHZ.

**D. Matlab command window output**

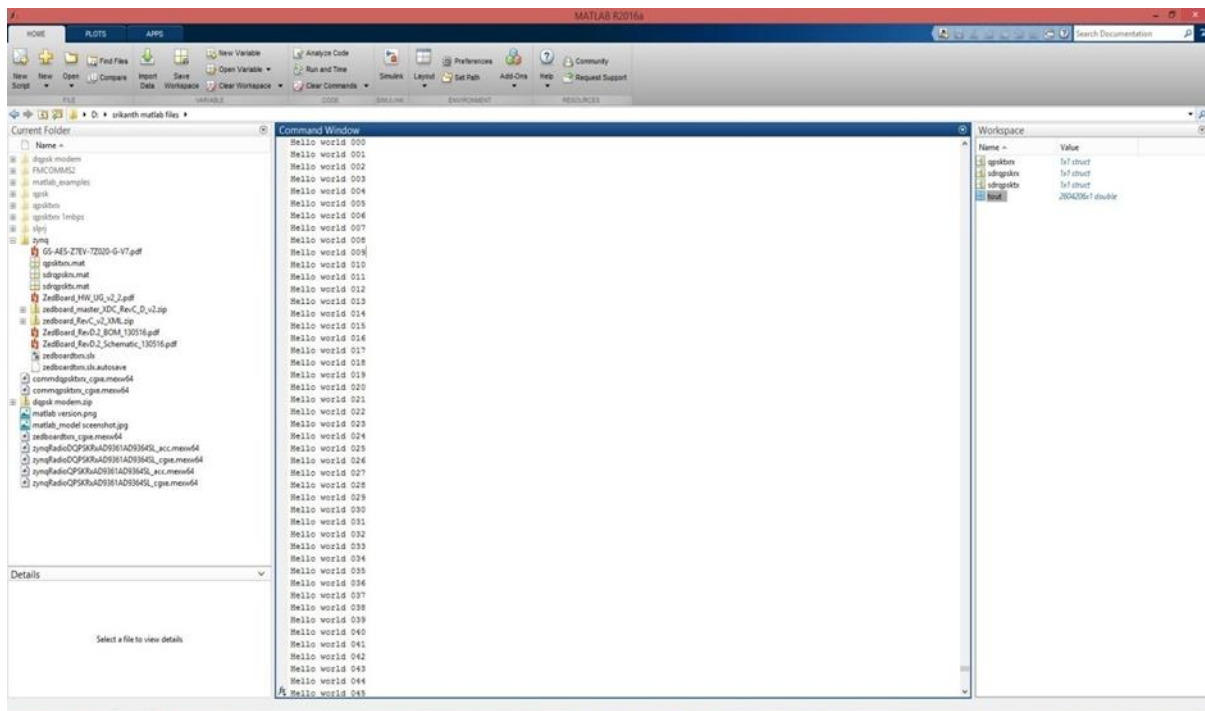
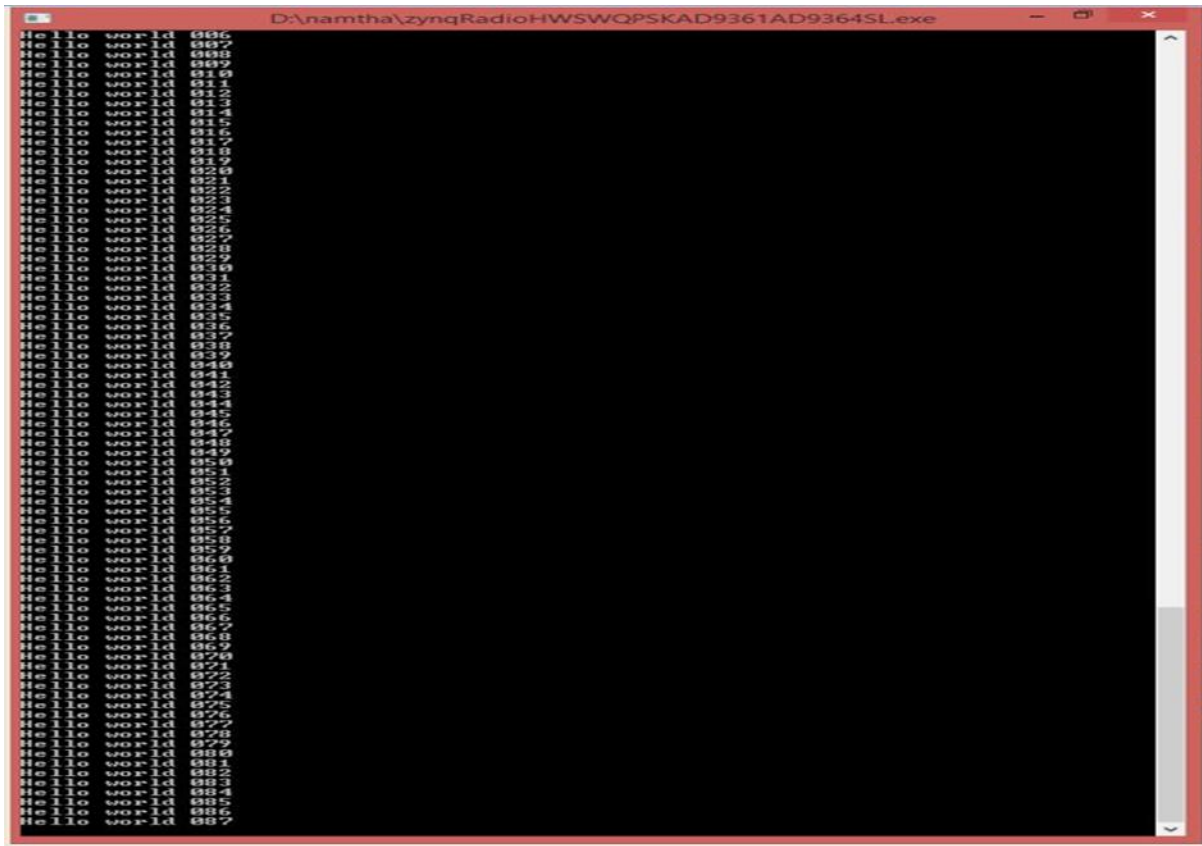
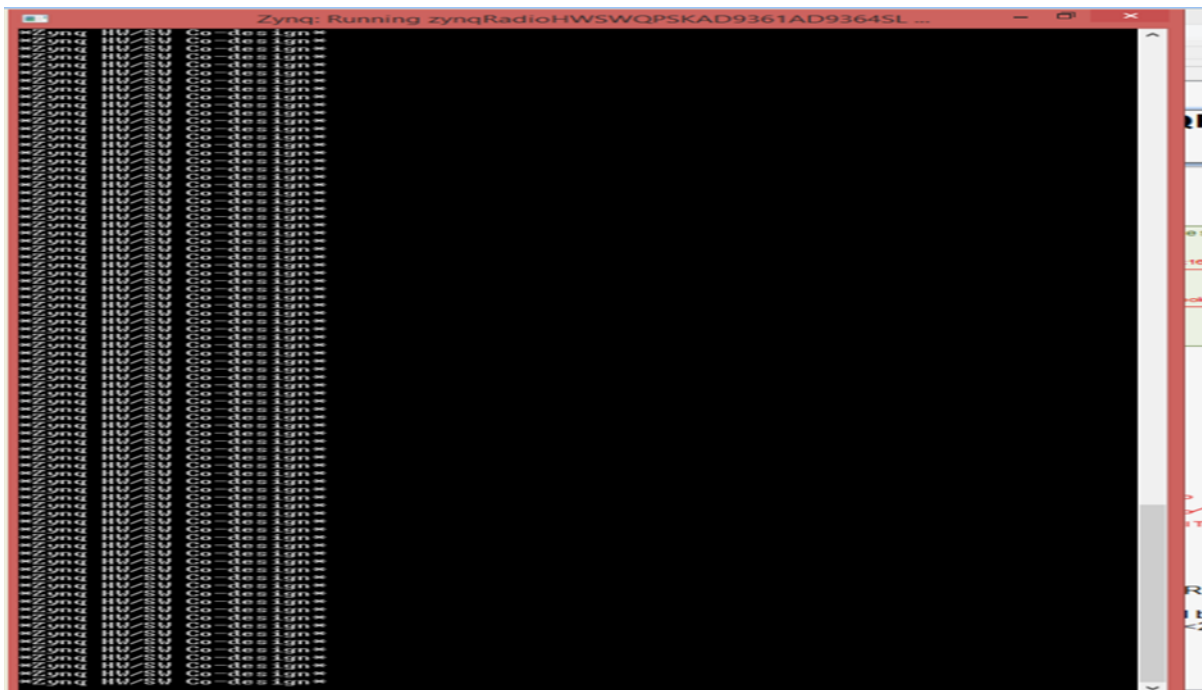


Fig 9: Transmitted message output in MATLAB Command window



```
D:\namtha\zynqRadio\HWSWQPSKAD9361AD9364SL.exe
Hello world 4996
Hello world 4997
Hello world 4998
Hello world 4999
Hello world 5000
Hello world 5001
Hello world 5002
Hello world 5003
Hello world 5004
Hello world 5005
Hello world 5006
Hello world 5007
Hello world 5008
Hello world 5009
Hello world 5010
Hello world 5011
Hello world 5012
Hello world 5013
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Hello world 5078
Hello world 5079
Hello world 5080
Hello world 5081
Hello world 5082
Hello world 5083
Hello world 5084
Hello world 5085
Hello world 5086
Hello world 5087
```

Fig 10: Command window output after generating HDL code when switch is connected to FPGA



```
Zynq: Running zynqRadioHWSWQPSKAD9361AD9364SL ...
Hello world 4996
Hello world 4997
Hello world 4998
Hello world 4999
Hello world 5000
Hello world 5001
Hello world 5002
Hello world 5003
Hello world 5004
Hello world 5005
Hello world 5006
Hello world 5007
Hello world 5008
Hello world 5009
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```

Fig 11: Command window output after generating HDL code when switch is connected to ARM

## 5. Conclusion

The direct conversion receiver is modeled and simulated using Zed board and ADFMCOMMS2-EBZ board. Direct conversion receiver translates RF signal to base band signal in one stage. The model drastically reduces cost, design time, board size, weight power and results in high performance. It also reduces the problem of image frequency. It is used to implement the digital modulation techniques. This model can be extended to  $\pi/4$  DQPSK modulation also.

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