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Enhancement Of Grid Power Quality By Using Dual Voltage Source Inverter

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ABSTRACT

This paper exhibits a double voltage source inverter (DVSI) plan to enhance the power quality and unwavering quality of the microgrid system. The proposed conspire is included two inverters, which empowers the microgrid to trade power produced by the conveyed vitality assets (DERs) and furthermore to repay the nearby unbalanced and nonlinear load. The control calculations are produced in view of instantaneous symmetrical component theory (ISCT) to work DVSI in lattice sharing and network infusing modes. The proposed plot has increased dependability, bring down data transmission prerequisite of the primary inverter, bring down cost because of decrease in filter size, and better use of small scale framework power while utilizing lessened dc-connect voltage rating for the principle inverter.

These components make the DVSI plot a promising choice for microgrid providing delicate loads. The topology and control calculation are approved through broad reenactment and trial comes about.

INTRODUCTION

Mechanical advance and natural concerns drive the power system to an outlook change with more sustainable power sources coordinated to the system by methods for conveyed era (DG). These DG units with coordinated control of nearby era and storerooms shape a microgrid [1]. In a microgrid, power from various sustainable power sources, for example, power modules, photovoltaic (PV) systems, and wind vitality systems are interfaced to framework and loads utilizing power electronic converters. A network intuitive inverter assumes an important part in trading power from the microgrid to the matrix and the associated load [2], [3]. This microgrid inverter can either work in a lattice sharing mode while providing a piece of neighborhood load or in matrix infusing mode, by infusing power to the principle framework.

Keeping up power quality is another important perspective which must be tended to while the microgrid system is associated with the primary network. The expansion of power gadgets and electrical loads with unbalanced nonlinear currents has debased the power quality in the power circulation net-work. Additionally, if there is a lot of feeder impedance in the circulation systems, the engendering of these consonant currents misshapes the voltage at the purpose of normal coupling (PCC). At a similar moment, industry mechanization has come to an abnormal state of modernity, where plants like car fabricating units, synthetic production lines, and semiconductor businesses require clean power. For these applications, it is fundamental to remunerate nonlinear and unbalanced load currents [4].Load pay and power infusion utilizing

matrix intuitive inverters in microgrid have been displayed in the writing [5], [6]. A solitary inverter system with power quality enhancement is talked about in [7]. The fundamental concentration of this work is to acknowledge double functionalities in an inverter that would give the dynamic power infusion from a solar PV system and furthermore fills in as a dynamic power filter, repaying unbalances and the receptive power required by different loads associated with the system.

In [8], a voltage direction and power flow control plot for a breeze vitality system (WES) is proposed. A circulation static compensator (DSTATCOM) is used for voltage direction and further more for dynamic power infusion. The control conspire keeps up the power balance at the network terminal amid the breeze varieties utilizing sliding mode control. A multifunctional power electronic converter for the DG power system is depicted in [9]. This plan has the ability to infuse power created by WES and furthermore to execute as a symphonious compensator. The vast majority of the reported writing around there talk about the topologies and control calculations to give load remuneration ability in a similar inverter notwithstanding their dynamic power infusion. At the point when a network associated inverter is utilized for dynamic power infusion and in addition for load pay, the inverter limit that can be used for accomplishing the second target is chosen by the accessible prompt microgrid genuine power [10].

Considering the instance of a network associated PV inverter, the accessible limit of the inverter to supply the responsive power turns out to be less amid the greatest solar insolation time frames [11]. At a similar moment, the responsive power to direct the PCC voltage is especially required amid this period [12]. It shows that giving multi functionalities in a solitary inverter corrupts either the genuine power infusion or the load pay capacities.

This paper exhibits a double voltage source inverter (DVSI) conspire, in which the power produced by the microgrid is infused as genuine power by the primary voltage source inverter (MVSI) and the receptive, consonant, and unbalanced load pay is performed by assistant voltage source inverter (AVSI). This has leeway that the evaluated limit of MVSI can simply be utilized to infuse genuine power to the network, if sufficient sustainable power is accessible at the dc interface. In the DVSI plot, as aggregate load power is provided by two inverters, power misfortunes over the semiconductor switches of every inverter are decreased. This increases its unwavering quality when contrasted with a solitary inverter with multifunctional abilities [13]

Additionally, littler size modular inverters can work at high switching frequencies with a lessened size of interfacing inductor, the filter cost gets decreased [14]. Besides, as the principle inverter is providing genuine power, the inverter needs to track the essential positive sequence of current. This decreases the data transmission necessity of the primary inverter. The inverters in the proposed conspire utilize two separate dc joins. Since the helper inverter is providing zero sequence of load current, a three-stage three-leg inverter topology with a solitary dc stockpiling capacitor can be utilized for the primary inverter. This thus decreases the dc-connect voltage prerequisite of the principle inverter. In this manner, the utilization of two separate inverters in the proposed DVSI plot gives increased unwavering quality, better use of microgrid power, diminished dc lattice voltage rating, less data transmission prerequisite of the fundamental inverter, and decreased filter measure [13]. Control calculations are produced by immediate symmetrical part hypothesis (ISCT) to work DVSI in framework associated mode, while considering non solid network voltage [15], [16].

The extraction of essential positive sequence of PCC voltage is finished by dq0 change [17]. The control technique is tried with two parallel inverters associated with a three-stage four-wire circulation system. Viability of the proposed control calculation is approved through itemized recreation and exploratory outcomes.

FACTS

Flexible AC Transmission Systems, called FACTS, got in the recent years a well known term for higher controllability in power systems by means of power electronic devices. Several FACTS-devices have been introduced for various applications worldwide. A number of new types of devices are in the stage of being introduced in practice.

In most of the applications the controllability is used to avoid cost intensive or landscape requiring extensions of power systems, for instance like upgrades or additions of substations and power lines. FACTS-devices provide a better adaptation to varying operational conditions and improve the usage of existing installations. The basic applications of FACTS-devices are:

- Power flow control,
- Increase of transmission capability,
- Voltage control,
- Reactive power compensation,
- Stability improvement,
- Power quality improvement,
- Power conditioning,
- Flicker mitigation,
- Interconnection of renewable and distributed generation and storages.

The utilization of lines for dynamic power transmission ought to be in a perfect world up to as far as possible. Voltage and stability limits should be moved with the methods for the few distinct FACTS gadgets. It can be seen that with developing line length, the opportunity for FACTS gadgets gets increasingly important.

The influence of FACTS-gadgets is accomplished through exchanged or controlled shunt remuneration, arrangement pay or stage move control. The gadgets work electrically as quick current, voltage or impedance controllers. The power electronic permits short response times down to far underneath one moment.

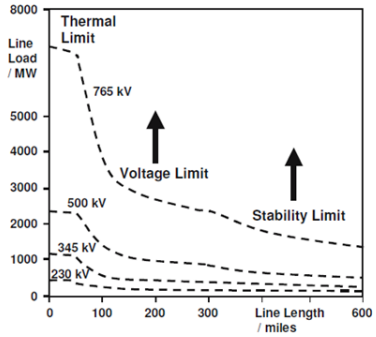

Figure 1: Operational limits of transmission lines for different voltage levels

The improvement of FACTS-gadgets has begun with the developing abilities of power electronic parts. Gadgets for high power levels have been made accessible in converters for high and even most noteworthy voltage levels. The general beginning stages are organize components influencing the receptive power or the impedance of a piece of the power system. Figure 2 demonstrates various fundamental gadgets isolated into the regular ones and the FACTS-gadgets.

For the FACTS side the scientific categorization as far as "dynamic" and "static" needs some clarification. The expression "dynamic" is utilized to express the quick controllability of FACTS-gadgets given by the power hardware. This is one of the principle separation factors from the customary gadgets. The expression "static" implies that the gadgets have no moving parts like mechanical changes to play out the dynamic controllability. In this manner a large portion of the FACTS-gadgets can similarly be static and dynamic.

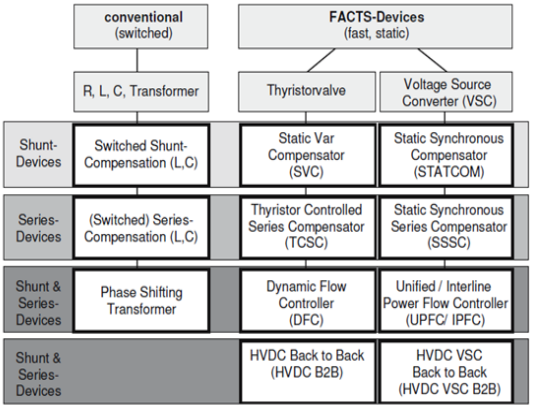

Figure 2: Major facts-Devices

The left segment in Figure 2 contains the ordinary gadgets work out of settled or mechanically switch capable parts like resistance, inductance or capacitance together with transformers. The FACTS-gadgets contain these components also yet utilize extra power electronic valves or converters to switch the components in littler strides or with switching designs inside a cycle of the rotating current. The left section of FACTS-gadgets utilizes Thyristor valves or converters. These valves or converters are outstanding since quite a long while. They have low misfortunes due to their low switching frequency of once a cycle in the converters or the use of the Thyristors to just scaffold impedances in the valves.

The correct segment of FACTS-gadgets contains more advanced innovation of voltage source converters construct today primarily in light of Insulated Gate Bipolar Transistors (IGBT) or Insulated Gate Commutated Thyristors (IGCT). Voltage Source Converters give a free controllable voltage in size and stage because of a heartbeat width regulation of the IGBTs or IGCTs. High tweak frequencies permit to get low sounds in the yield flag and even to remunerate disturbances originating from the system. The burden is that with an increasing switching frequency, the misfortunes are increasing also. Subsequently exceptional plans of the converters are required to repay this.

OPERATING PRINCIPLE OF UPFC

The essential segments of the UPFC are two voltage source inverters (VSIs) sharing a typical dc stockpiling capacitor, and associated with the power system through coupling transformers. One VSI is associated with in shunt to the transmission system by means of a shunt transformer, while the other one is associated in arrangement through an arrangement transformer.

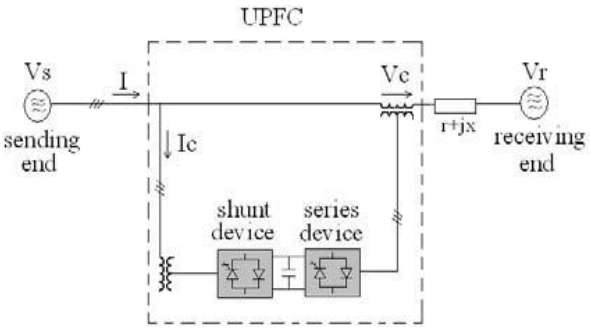

Figure 3: A basic UPFC functional scheme

The arrangement inverter is controlled to infuse a symmetrical three stage voltage system (Vse), of controllable greatness and stage point in arrangement with the line to control dynamic and responsive power streams on the transmission line. Thus, this inverter will trade dynamic and responsive power with the line. The responsive power is electronically given by the arrangement inverter, and the dynamic power is transmitted to the dc terminals. The shunt inverter is worked so as to request this dc terminal power (positive or negative) from the line keeping the voltage over the capacity capacitor Vdc steady. Thus, the net genuine power retained from the line by the UPFC is equivalent just to the misfortunes of the inverters and their transformers. The rest of the limit of the shunt inverter can be utilized to trade responsive power with the line so to give a voltage control at the association point.

The two VSI's can work autonomously of each other by isolating the dc side. So all things considered, the shunt inverter is working as a STATCOM that

produces or assimilates receptive power to manage the voltage extent at the association point. Rather, the arrangement inverter is working as SSSC that produces or assimilates receptive power to control the current stream, and hence the power low on the transmission line.

The UPFC has numerous conceivable working modes. Specifically, the shunt inverter is working in such an approach to infuse a controllable current, ish into the transmission line. The shunt inverter can be controlled in two unique modes:

VAR Control Mode: The reference input is an inductive or capacitive VAR request. The shunt inverter control translates the var reference into a corresponding shunt current request and adjusts gating of the inverter to establish the desired current. For this mode of control a feedback signal representing the dc bus voltage, Vdc, is also required.

Automatic Voltage Control Mode: The shunt inverter reactive current is automatically regulated to maintain the transmission line voltage at the point of connection to a reference value. For this mode of control, voltage feedback signals are obtained from the sending end bus feeding the shunt coupling transformer.

The series inverter controls the magnitude and angle of the voltage injected in series with the line to influence the power flow on the line. The actual value of the injected voltage can be obtained in several ways.

Direct Voltage Injection Mode: The reference inputs are directly the magnitude and phase angle of the series voltage.

Phase Angle Shifter Emulation mode: The reference input is phase displacement between the sending end voltage and the receiving end voltage. Line Impedance Emulation mode: The reference input is an impedance value to insert in series with the line impedance

Automatic Power Flow Control Mode: The reference inputs are values of P and Q to maintain on the transmission line despite system changes.

DUAL VOLTAGE SOURCE INVERTER

System Topology

The proposed DVSI topology is shown in Fig.4. It consists of a neutral point clamped (NPC) inverter to realize AVSI and a three-leg inverter for MVSI[18].These are connected to grid at the PCC and supplying a nonlinear and unbalanced load. The function of the AVSI is to compensate there active, harmonics, and unbalance components in load currents. Here, load currents in three phases are represented by i_{la},i_{lb}, and i_{lc}, respectively. Also, $i_{g(abc)}$,$i_{\mu gm(abc)}$, and $i_{\mu gx(abc)}$ show grid currents, MVSI currents, and AVSI currents in three phases, respectively. The dc link of the AVSI utilizes a split capacitor topology, with two capacitors C_1 and C_2.The MVSI delivers the available power at distributed energy resource (DER) to grid. The DER can be a dc source or an ac source with rectifier coupled to dc link. Usually, renewable energy sources like fuel cell and PV generate power at variable low dc voltage, while the variable speed wind turbines generate power at variable ac voltage. Therefore, the power generated from these sources use a power conditioning stage before it is connected to the input of MVSI. In this study, DER is being represented as a dc source. An inductor filter is used to eliminate the high-frequency switching components generated due to the switching of power electronic switches in the inverters [19]. The system considered in this study is assumed to have some amount of feeder resistance R_g and inductance L_g. .

Due to the presence of this feeder impedance, PCC voltage is affected with harmonics [20]. Section III describes the extraction of fundamental positive sequence of PCC voltages and control strategy for the reference current generation of two inverters in DVSI scheme.

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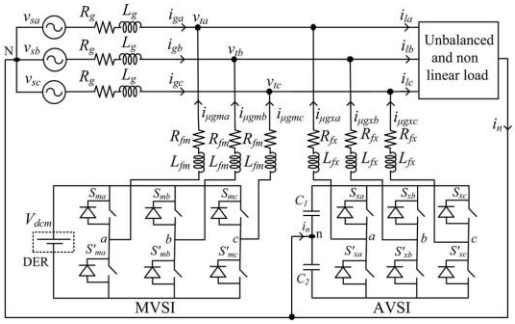

Figure 4: The proposed DVSI topology

Design of DVSI Parameters

1) AVSI: The important parameters of AVSI like dc-link voltage(V_{dc}), dc storage capacitors(C_1 and C_2),interfacing inductance(L_{fx}), and hysteresis band($\pm h_x$) are selected based on the design method of split capacitor DSTATCOM topology[16]. The dc-link voltage across each capacitor is taken as1.6 times the peak of phase voltage. The total dc-link voltage reference (V_{dcref}) is found to be 1040V.

Values of dc capacitors of AVSI are chosen based on the change in dc link voltage during transients. Let total load rating is *S* kVA. In the worst case, the load power may vary from minimum to maximum, i.e., from 0 to *S* kVA. AVSI needs to exchange real power during transient to maintain the load power demand. This transfer of real power during the transient will result in deviation of capacitor voltage from its reference value. Assume that the voltage controller takes *n* cycles, i.e., *nT* seconds to act, where *T* is the system time period. Hence, maximum energy exchange by AVSI during transient will be *nST*. This energy will be equal to change in the capacitor stored energy.

Therefore

$$\frac{1}{2}c_1(V_{dcr}^2 - V_{dc1}^2) = nST \_\_\_\_\_(1)$$

Where V_{dcr} and V_{dc1} are the reference dc voltage and maximum permissible dc voltage across C_1 during transient, respectively. Here, S= 5kVA, V_{dcr}=520V, V_{dc1}=0.8∗V_{dcr} or 1.2∗V_{dcr}, n=1, and T=0.02s. Substituting these values in (1), the dc- link capacitance (C_1) is calculated to be 2000μF. Same value of capacitance is selected for C_2.

The interfacing inductance is given by

$$L_f = \frac{1.6V_m}{4h_x f_{max}} \text{ -------- (2)}$$

Assuming a maximum switching frequency (f_{max}) of 10kHz and hysteresis band (h_x) as 5% of load current (0.5A),the value of L_{fx} is calculated to be 26mH.

2) MVSI : The MVSI uses a three-leg inverter topology. Its dc-link voltage is obtained as 1.15∗V_{ml}, where V_{ml} is the peak value of line voltage. This is calculated to be 648V. Also, MVSI Supplies a balanced sinusoidal current at unity power factor. So, zero sequence switching harmonics will be absent in the output current of MVSI. This reduces the filter requirement for MVSI as compared to AVSI[21]. In this analysis, a filter inductance (L_{fm}) of 5mH isused.

ADVANTAGES OF THE DVSI SCHEME :

The various advantages of the proposed DVSI scheme over a single inverter scheme with multifunctional capabilities [7]–[9] are discussed here as follows:

1) Increased Reliability: DVSI scheme has increased reliability, due to the reduction in failure rate of components and the decrease in system down time cost [13]. In this scheme, the total load current is shared between AVSI and MVSI and hence reduces the failure rate of inverter switches. Moreover, if one inverter fails, the other can continue its operation. This reduces the lost energy and hence the down time cost. The reduction in system down time cost improves the reliability.

2) Reduction in Filter Size: In DVSI scheme, the current supplied by each inverter is reduced and hence the current rating of individual filter inductor reduces.

This reduction in current rating reduces the filter size. Also, in this scheme, hysteresis current control is used to track the inverter reference currents. As given in (2), the filter inductance is decided by the inverter switching frequency. Since the lower current rated semicon- ductor device can be switched at higher switching frequency, the inductance of the filter can be lowered. This decrease in inductance further reduces the filter size.

3) Improved Flexibility: Both the inverters are fed from separate dc links which allow them to operate independently, thus increasing the flexibility of the system. For instance, if the dc link of the main inverter is disconnected from the system, the load compensation capability of the auxiliary inverter can still be utilized.

4) Better Utilization of Microgrid Power: DVSI scheme helps to utilize full capacity of MVSI to transfer the entire power generated by DG units as real power to ac bus, as there is AVSI for harmonic and reactive power compensation. This increases the active power injection capability of DGs in microgrid [22].

5) Reduced DC-Link Voltage Rating: Since, MVSI is not delivering zero sequence load current components, a single capacitor three-leg VSI topology can be used. Therefore, the dc- link voltage rating of MVSI is reduced approximately by 38%, as compared to a single inverter system with split capacitor VSI topology.

CONTROL STRATEGY FOR DVSI SCHEME

A. Fundamental Voltage Extraction

The control algorithm for reference current generation using ISCT requires balanced sinusoidal PCC voltages. Because of the presence of feeder impedance, PCC voltages are distorted. Therefore, the fundamental positive sequence components of the PCC voltages are extracted for the reference current generation. To convert the distorted PCC voltages to balanced

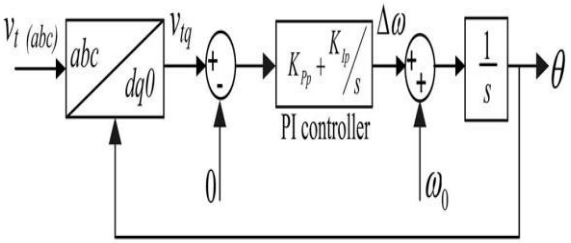

Figure 5: Schematic diagram of PLL

Sinusoidal voltages, $dq0$ transformation is used. The PCC voltages in natural reference frame (v_{ta},v_{tb},andv_{tc}) are first transformed into $dq0$ reference frame as given by

$$\begin{bmatrix} v_{td} \\ v_{tq} \\ v_{to} \end{bmatrix} = C \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \text{ ---------- (3)}$$

Where

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

In order to get θ, a modified synchronous reference frame(SRF) phase locked loop(PLL)[23] isused. The schematic diagram of this PLL is shown in Fig.5. It mainly consists of a proportional integral(PI) controller and an integrator. In this PLL, the SRF terminal voltage in q-axis(v_{tq}) is compared with 0V and the error voltage thus obtained is given to the PI controller. The frequency deviation $\Delta\omega$is then added to the reference frequency ω_0 and finally given to the integrator to get θ. It can be proved that, when, $\theta=\omega_0 t$ and by using the Park's transformation matrix(C),q-axis voltage in $dq0$ frame becomes zero and hence the PLL will be locked to the reference Frequency (ω_0). As PCC voltages are distorted, the transformed voltages in $dq0$ frame(v_{td} and

v_{tq}) contain average and oscillating components of voltages. These can be represented as :

$$v_{td} = \bar{v}_{td} + \tilde{v}_{td},\ v_{tq} = \bar{v}_{tq} + \tilde{v}_{tq} \text{--- (4)}$$

Instantaneous Symmetrical Component Theory :

ISCT was developed primarily for unbalanced and nonlinear load compensations by active power filters. The system topology shown in Fig.6.is used for realizing the reference current for the compensator [15]. The ISCT for load compensation is derived based on the following three conditions.

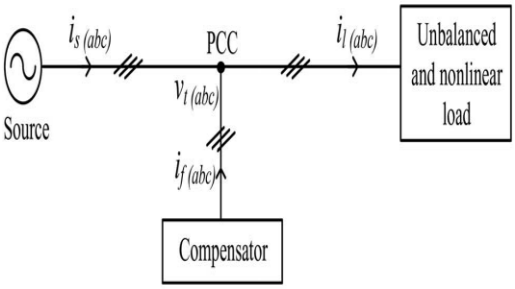

Fig.6. Schematic of an unbalanced and nonlinear load compensation scheme

1) The source neutral current must be zero. Therefore

$$i_{sa} + i_{sb} + i_{sc} = 0. \text{ ---------- (5)}$$

2) The phase angle between the fundamental positive sequence voltage (v+ ta1) and source current (isa) is φ

$$\angle v_{ta1}^{+} = \angle i_{sa} + \emptyset \text{ ---------- (6)}$$

3) The average real power of the load (Pl) should be supplied by the source

$$v_{ta1}^{+} i_{sa} + v_{tb1}^{+} i_{sb} + v_{tc1}^{+} i_{sc} = P_t. \text{ ------ (7)}$$

Solving the above three equations, the reference source currents can be obtained as

$$\left.\begin{aligned} i_{sa}^{*} &= \left(\frac{v_{ta1}^{+} + \beta(v_{tb1}^{+} - v_{tc1}^{+})}{\Sigma_{j=a,b,c} \angle_{tj}^{+\,2}}\right) P_t \\ i_{sb}^{*} &= \left(\frac{v_{tb1}^{+} + \beta(v_{tc1}^{+} - v_{ta1}^{+})}{\Sigma_{j=a,b,c} v_{tj}^{+\,2}}\right) P_t \\ i_{sc}^{*} &= \left(\frac{v_{tc1}^{+} + \beta(v_{ta1}^{+} - v_{tb1}^{+})}{\Sigma_{j=a,b,c} v_{tj}^{+\,2}}\right) P_t \end{aligned}\right\} \text{ (8)}$$

The term φ is the desired phase angle between the fundamental positive sequence of PCC voltage and source current. To achieve unity power factor for source current, substitute β =0in (9). Thus, the reference source currents for three phases are given by

$$i_{s(abc)}^{*} = \left(\frac{v_{t(abc)1}^{+}}{\Sigma_{j=a,b,c} v_{tj}^{+\,2}}\right) P_t \text{ ---------- (9)}$$

Where i_{sa}, i_{sb}, $i_{sc}$are fundamental positive sequence of load currents drawn from the source, when it is supplying an average load power P_t and can be computed using a moving average filter with a window of one-cycle data points as given below

$$P_t = \frac{1}{T}\int_{t_1-T}^{t_1} (v_{ta1}^{+} i_{la} + v_{tb1}^{+} i_{lb} + v_{tc1}^{+} i_{lc}) dt$$
---------- (10)

Where t1 is any arbitrary time instant. Finally, the reference currents for the compensator can be generated as follows:

$$i_{f\,(abc)}^{*} = i_{f\,(abc)} - i_{s\,(abc)}^{*} \text{---------- (11)}$$

Equation (12) can be used to generate the reference filter currents using ISCT, when the entire load active power, P_t is supplied by the source and load compensation is performed by a single inverter. A modification in the control algorithm is required, when it is used for DVSI scheme. The following section discusses the formulation of control algorithm for DVSI scheme. The source currents, $i_{s(abc)}$ and filter currents $i_{f(abc)}$ will be equivalently represented as grid currents $i_{g(abc)}$ and AVSI currents $i_{\mu gx(abc)}$, respectively, in further sections.

Control Strategy of DVSI

Control strategy of DVSI is created such that network and MVSI together offer the dynamic load power, and AVSI supplies rest of the power parts requested by the load.

Reference Current Generation for Auxiliary Inverter: The dc-link voltage of the AVSI should be maintained constant for proper operation of the auxiliary inverter. DC-link voltage variation occurs in auxiliary inverter due to its switching and ohmic losses. These losses termed as Ploss. should also be supplied by the grid. An expression for Ploss is derived on the condition that average dc capacitor current is zero to maintain a constant capacitor voltage [15]. The deviation of average capacitor current from zero wills reflect as a change in capacitor voltage from a steady state value. A PI controller is used to generate P loss term is given as:

$$P_{loss} = K_{Pv} e_{vdc} + K_{Iv} \int e_{vdc}\, dt \text{ ------(12)}$$

The Ploss term thus obtained should be supplied by the grid, and therefore AVSI reference currents can be obtained as given in (14). Here, the dc-link voltage PI controller gains are selected so as to ensure stability and better dynamic response during load change [24].

$$\left.\begin{aligned} i^*_{\mu gxa} &= i_{la} - \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+\,2}_{tj}}\right)(P_t + P_{loss}) \\ i^*_{\mu gxb} &= i_{lb} - \left(\frac{v^+_{tb1}}{\sum_{j=a,b,c} v^{+\,2}_{tj}}\right)(P_t + P_{loss}) \\ i^*_{\mu gxc} &= i_{lc} - \left(\frac{v^+_{tc1}}{\sum_{j=a,b,c} v^{+\,2}_{tj}}\right)(P_t + P_{loss}) \end{aligned}\right\} \quad (13)$$

Reference Current Generation for Main Inverter: The MVSI supplies balanced sinusoidal currents based on the available renewable power at DER. If MVSI losses are neglected, the power injected to grid will be equal to that available at DER (Pug).The following equation, which is derived from ISCT can be used to generate MVSI reference currents for three phases (a, b, and c).

$$i^*_{\mu gm(abc)} = \left(\frac{v^+_{t(abc)1}}{\sum_{j=a,b,c} v^{+\,2}_{tj}}\right) P_{\mu g} \quad \text{----- (14)}$$

where Pµg is the available power at the dc link of MVSI.

The reference currents obtained from (14) to (15) are tracked by using hysteresis band current controller (HBCC). HBCC schemes are based on a feedback loop, usually with a two-level comparator.

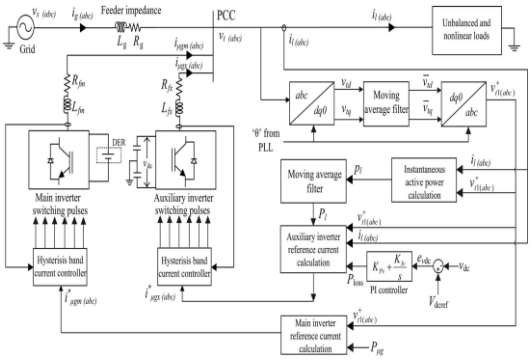

Figure 7: The schematic diagram of Control strategy of the proposed DVSI Scheme

This controller has the advantage of peak current limiting capacity, good dynamic response, and simplicity in implementation [14]. A hysteresis controller is a high-gain proportional controller. This controller adds certain phase lag in the operation based on the hysteresis band and will not make the system unstable. Also, the proposed DVSI scheme uses a first-order inductor filter which retains the closed-loop system stability [25]. The entire control strategy is schematically represented in Fig.7. Applying Kirchoff's current law (KCL) at the PCC in Fig. 7.

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$$i_{\mu g x\, j} = i_{l\, j} - \left(i_{g\, j} + i_{\mu g m\, j}\right), \quad \text{for j=a,b,c.}$$
---------- (15)

By using above equations an expression for reference grid current in phase-a (i∗ga) can be obtained as

$$i^*_{ga} = \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)[(P_l + P_{loss}) - P_{\mu g}]$$
-------- (16)

SIMULATION STUDIES

The simulation model of DVSI plot appeared in Fig. 1is created in PSCAD 4.2.1 to assess the performance. The simulation parameters of the system. The simulation think about shows the lattice sharing and grid injecting methods of operation of DVSI plot in unfaltering state and in addition in transient conditions.

The contorted PCC voltages because of the feeder impedance without DVSI conspire are appeared in Fig. 5(a). On the off chance that these distorted voltages are utilized for the reference current era of AVSI, the current pay won't be appropriate [14]. Accordingly, the crucial positive sequence of voltages is removed from these twisted voltages utilizing the calculation. These separated voltages are given in Fig. 5(b). These voltages are additionally utilized for the era of inverter reference currents. Fig. 6(a)–(d) speaks to dynamic power requested by load (P)

Parameters	Values
Grid voltage	400 V(L–L)
Fundamental frequency	50 Hz
Feeder impedance	R_g = 0.5 Ω, L_g = 1.0 mH
AVSI	$C_1 = C_2$ = 2000 μF V_{dcref} = 1040 V Interfacing inductor, L_{fx} = 20 mH Inductor resistance, R_{fx} = 0.25 Ω Hysteresis band ($\pm h_x$) = 0.1 A
MVSI	DC-link voltage, V_{dcm} = 650 V Interfacing inductor, L_{fm} = 5 mH Inductor resistance, R_{fm} = 0.25 Ω Hysteresis band ($\pm h_m$) = 0.1 A
Unbalanced linear load	Z_{la} = 35 + j19 Ω Z_{lb} = 30 + j15 Ω Z_{lc} = 23 + j12 Ω
Nonlinear load	3 ϕ diode bridge rectifier with DC side current of 3.0 A
DC voltage controller gains	K_{Pv} =10, K_{Iv} = 0.05

Micro grid is operating in grid sharing mode At t=0.4s, the micro grid power is increased to7kW, which is more than the load demand of 6kW.This microgrid power change is considered to show the change of operation of MVSI from grid sharing to grid injecting mode. Now, the excess power of 1kW is injected to the grid and hence, the power drawn from grid is shown as negative. Fig.14(b) shows The load reactive power (QI), reactive power supplied by AVSI(Q_X),and reactive power supplied by MVSI ($Q_{\mu g}$), respectively. It shows that to load reactive power is supplied by AVSI, as expected.

The Fig.13. shows the plots of load currents($i_{l(abc)}$), currents drawn from grid($i_{g(abc)}$), currents drawn from MVSI ($i_{\mu g(abc)}$), and currents drawn from the AVSI ($i_{\mu x(abc)}$), respectively. The load currents are unbalanced and distorted respectively. The load currents are unbalanced and distorted. The MVSI supplies a balanced and sinusoidal current during grid supporting and grid injecting modes. The currents drawn from grid are also perfectly balanced and sinusoidal, as the auxiliary inverter compensates the unbalance and harmonics.

The MVSI supplies a balanced and sinusoidal currents during (iga) during grid sharing and grid injecting modes. During grid sharing mode, this PCC voltage and grid current are in phase and during grid injecting mode, they are out of phase. The same is true for other two phases. Thus the compensation capability of AVSI makes the source current and MVSI current at unity power factor operation.

The dc-link voltage of AVSI is shown in Fig.13. These figures indicate that the voltage is maintained constant at a reference voltage (Vdcref) of 1040 V by the PI controller. All these simulation results pre-sented above demonstrate the feasibility of DVSI for the load compensation as well as power injection from DG units in a microgrid.

EXPERIMENTAL RESULTS

The performance of the proposed DVSI is verified with experimental studies. A digital signal processor (DSP)-based prototype of DVSI has been developed in the laboratory. The experimental system parameters are given in Table II. The setup consists of two 10 kVA SEMIKRON build two-level inverter for realizing AVSI and MVSI. A DSP TMS320F28335 is used to process the data in digital domain with a sampling time of 19.5 μs. The signal and logic level circuit consist of Hall effect voltage and current transducers, signal conditioning, and protection circuits along with isolated dc power supplies. A real time algorithm has been implemented in code composer studio (CCS) on the host computer. The DSP acquires the signals and processes them to generate reference currents for AVSI and MVSI. The switching commands generated by the DSP are then issued to inverters through its general purpose input and output ports.

Tests are conducted to verify the operation of DVSI during steady state as well as transient with a sudden load change. The three phase PCC voltages(Vt(abc)) are shown in Fig.12. From these distorted PCC voltages, fundamental positive sequence voltages are extracted using the algorithm. These voltages are further used for realizing AVSI and MVSI reference currents. A software PLL which is implemented in DSP is being used for this extraction. The reference power of MVSI($P_{\mu g}$) has been set at 300W.The total unbalanced and nonlinear load considered in this study take an average real power of 500W and a reactive power of 260VAr.The phase-*a* PCC voltage and three phase load currents before compensation are shown in Fig.13.The PCC voltages and grid currents after compensation are showninFig.14(a). It indicates that the compensated grid currents become balanced sinusoidal and are in phase with the respective PCC voltages. Fig.14(b) represents MVSI currents and dc-link voltage and AVSI currents. From these two figures, it is observed that MVSI currents are balanced sinusoidal and at unity power factor with respective PCC voltages and AVSI supplies the unbalance, harmonic and reactive components of load currents.

The dynamic performance of the AVSI is illustrated by displaying load currents, filter currents, source currents, and dc-link voltage as in Fig.12&13.The load changes from unbalanced and nonlinear to balanced nonlinear load at an instant $t1$.The AVSI begins to compensate the load instantaneously. The grid and filter currents settle within half a cycle. At the instant $t2$, the load changes back to its normal value. The source and filter currents again settle within a cycle. The rise and fall in dc-link voltage due to the sudden decrease and increase in load is not visible in the graph. This is because, the dc-link voltage control loop is slow and takes few cycles to settle down. Grid current transient during the change of operation of MVSI from grid injecting to grid sharing mode. It is considered that MVSI supplies 300W during entire operation. A linear unbalanced load which takes an active power of 140W is supplied by the DVSI until the time $t1$.Therefore, the remaining micro grid power of about 160W is injected to grid. At the instant $t1$, the load changes to unbalanced and nonlinear which consumes an average power of 500W.Therefore, beyond $t1$, an active power of 200W is supplied from grid. This figure shows that unity power factor for grid current is achieved during grid injecting and grid sharing modes of operation.

Simulation Models and Results :

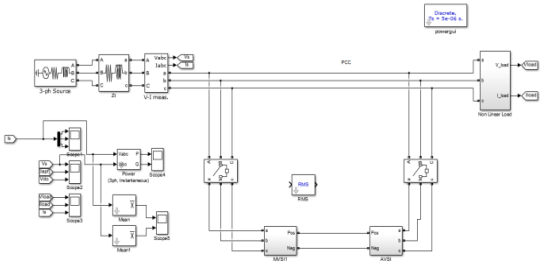

Fig.8 DVSI Main circuit

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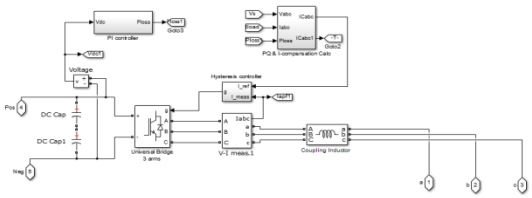

Fig.9 Main Voltage source Inverter sub system

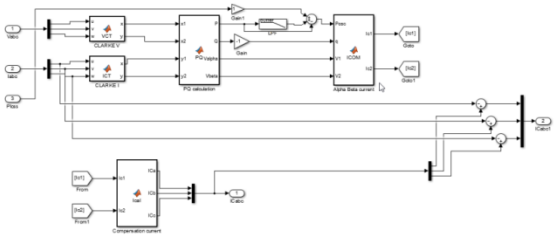

Figure 10: control diagram

SIMULATION RESULTS:

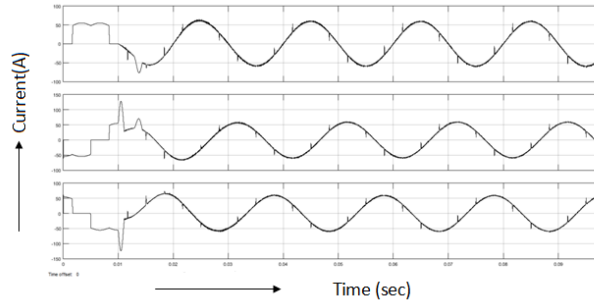

Figure 11: Source Current

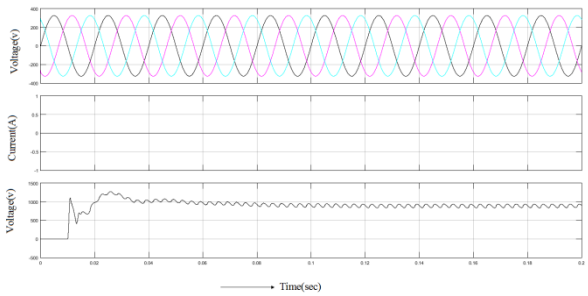

Figure 12: Source Voltage, Filter Current and DC Voltage

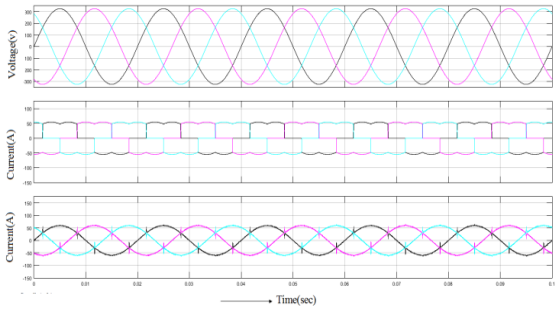

Figure 13: Load Voltage, load Current and Source Current

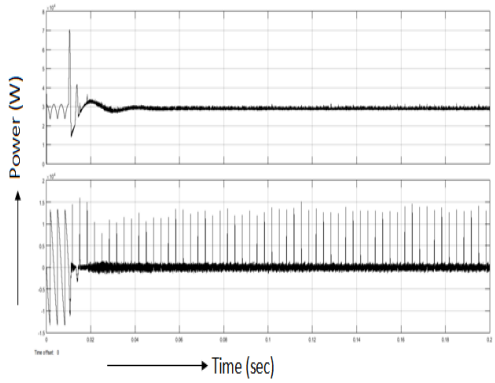

Figure 14: a) ACTIVE POWER and
b) REACTIVE POWER

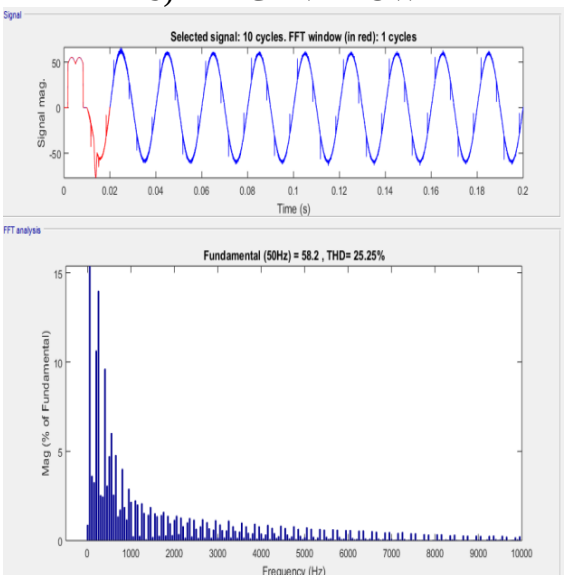

Figure 15: THD before DVSI

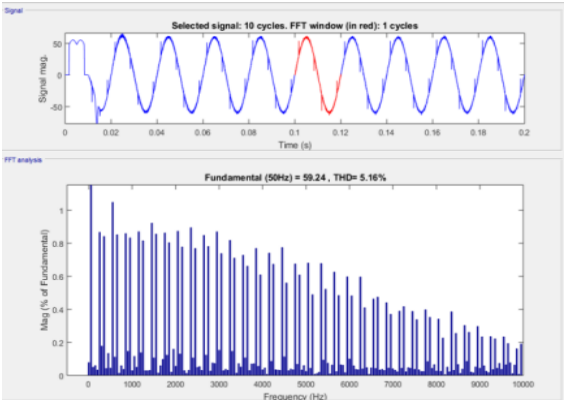

Figure 16: THD after DVSI

CONCLUSION:

A DVSI plot is proposed for microgrid systems with enhanced power quality. Control calculations are created to produce reference currents for DVSI utilizing ISCT. The proposed conspire has the capacity to trade power from conveyed generators (DGs) and furthermore to repay the nearby unbalanced and nonlinear load. The performance of the proposed plot has been approved through simulation and exploratory examinations. When contrasted with a solitary inverter with multifunctional abilities, a DVSI has many points of interest, for example, increased dependability, bring down cost because of the decrease in filter size, and more use of inverter ability to infuse genuine power from DGs to microgrid. In addition, the utilization of three-stage, three-wire topology for the principle inverter lessens the dc-interface voltage necessity. Consequently, a DVSI conspire is a reasonable interfacing choice for microgrid providing touchy loads.

FUTURE SCOPE

Power Quality is enhanced by utilizing DVSI and we are lessen the music and wipe out the misfortunes in the transmission line. What's more, the voltage is created in the system by utilizing PWM procedure. The created voltage is nonlinear or unbalance in the three stage line. along these lines, this nonlinear or unbalance in the three stage line so this non straight condition is balanced or controlled by utilizing whatever other strategies additionally, as multlivel inverters or by using advanced techniques like fluffy, neurol rationales or even with streamlining procedures like hereditary calculation, molecule swaram enhancement.

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