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Design of Dynamic Comparators using Tanner EDA Tools

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Abstract:

A replacement absolutely differential CMOS dynamic comparator victimization feedback appropriate for pipeline A/D converters with low power dissipation, low offset, low noise and high speed is proposed. Inputs square measure reconfigured from typical differential try comparator specified close to equal current distribution within the input transistors may be achieved for a meta stable purpose of the comparator. Restricted signal swing clock for the tail current is additionally wont to guarantee constant currents within the differential pairs. Nearly 18mV offset voltage is definitely achieved with the proposed structure creating it favorable for flash and pipeline conversion applications.

The projected topology is predicated on 2 cross coupled differential pairs positive feedback and switchable current sources, encompasses a little power dissipation, less physical phenomenon band, less area, and it's shown to be terribly sturdy against semiconductor device pair, noise immunity. Implementation of the comparators, designed in GPDK 90 nm square measure measured to see offset power dissipation and speed with 1.8 V square measure compared and also the superior options of the projected comparator square measure established.

Keywords—**CMOS, PMOSFET, NMOSFET, CMOS comparator, TIQ comparator, low power, differential comparator, CMOS-LTE, TANNER TOOL S-edit, L-edit, W-edit**

Introduction

The basic and schematic operation of a voltage comparator square measure shown in fig1, this comparator is often thought of as a choice creating circuit.

Definition:- The comparator may be a circuit that compares associate degree analog signal with another analog signal or reference and outputs a binary signal supported the comparison. If the $+V_P$, the input of the comparator is at a maximum potential than the $-V_N$, input, the output of the comparator may be a logic one, wherever as if the + input is at a possible but the – input, the output of the comparator is at logic zero.

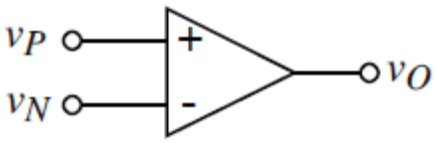

Fig. 1: Symbol of a Comparator

Dynamic Comparator Design:

A totally differential typical dynamic comparator is shown in fig.5.1. The comparator consists of 2 cross coupled differential pairs with electrical converter latch at the highest. Comparison is formed supported the electrical converter currents, that square measure associated with the inputs, once the Øclk goes high. The trip purpose may be modified by acceptable input semiconductor device size . Few points square measure price noting in reference to the issues gift during this structure. the primary downside of traditional differential comparator is expounded to the continuance of the tail current. once clock signal goes high, the tail current can move into linear region and can be perform of the inputs of the individual differential combine. If there square measure any non-idealities or mismatches gift (from the purpose read of symmetry), the 2 electrical converter tail currents won't be same and can lead to giant offset for the comparator. The second drawback is expounded to the inputs of a differential combine. an oversized distinction between the 2 inputs to a differential combine can lead to the turning of 1 of the differential combine MOSFET and every one of the tail current[3] are going to be drawn into the opposite MOSFET. Hence, in impact comparator are going to be solely scrutiny Vin+ with Vref+ (or Vin- with Vref-) instead of a comparison of differential Vin with differential Vref . The third potential

drawback related to the previous code dependent biased call. this will happen if there's some charge imbalance left from previous call at one in every of the nodes of the comparator which might have an effect on next call. to beat the drawbacks of the everyday differential combine comparator, a brand new dynamic comparator has been projected within the next section that addresses the on top of listed issues.

Dynamic Comparator Operation

When the comparator is inactive the clk is at terrorist organization, means the present supply transistors NM6 and NM7are changed and no current path between the availability voltages exists. at the same time the PMOS switch transistors PM1 and PM4 reset the outputs by shorting them to Vdd. The NMOS transistors NM0 and NM1 of the latch conduct and force additionally the drains of all the input transistors NM2 – NM5 to Vdd potential. once clk is up to Vdd ,the outputs square measure disconnected from the positive offer and also the switch current sources NM6 and NM7 enter saturation and start to conduct. The wave shape of the Dynamic comparator is shown. Here the given reference voltage as 500mV.So below 500mV it ought to offer logic0. And once reference Voltage it ought to offer logic1.And sweeping the input Voltage as -1V to 1.8V.The wave kind of the Dynamic comparator is shown in Fig.2**.**

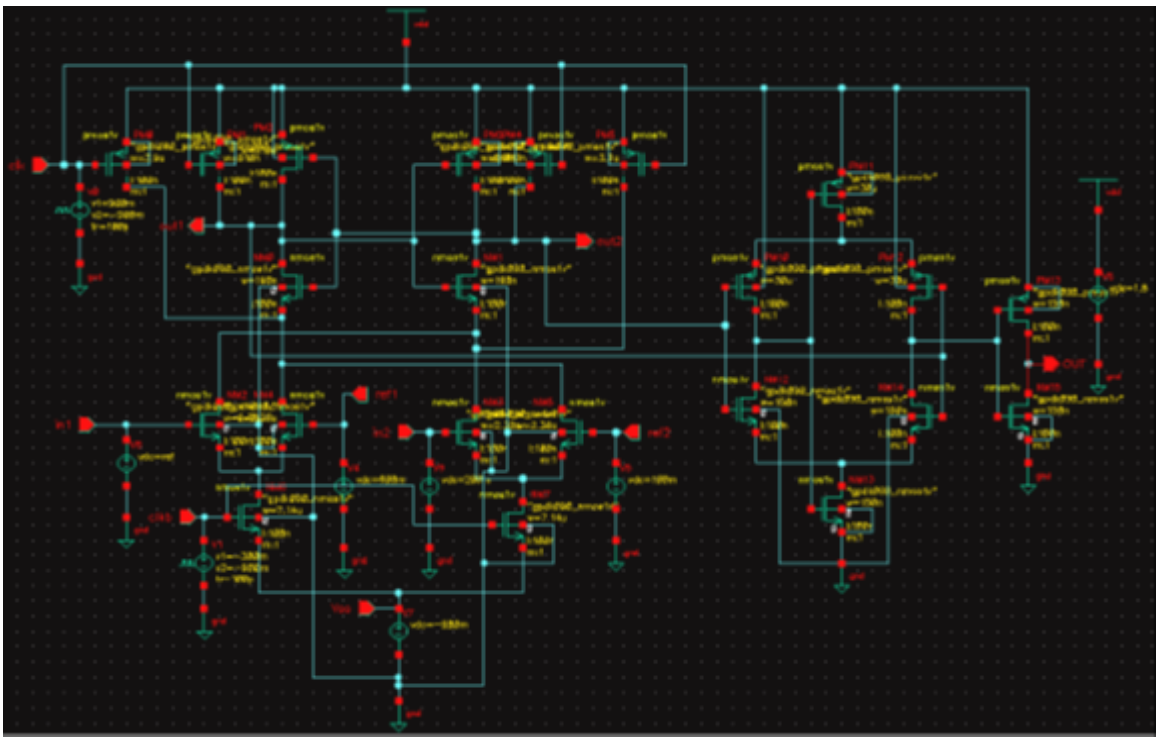

Fig.2 .Dynamic comparator circuit

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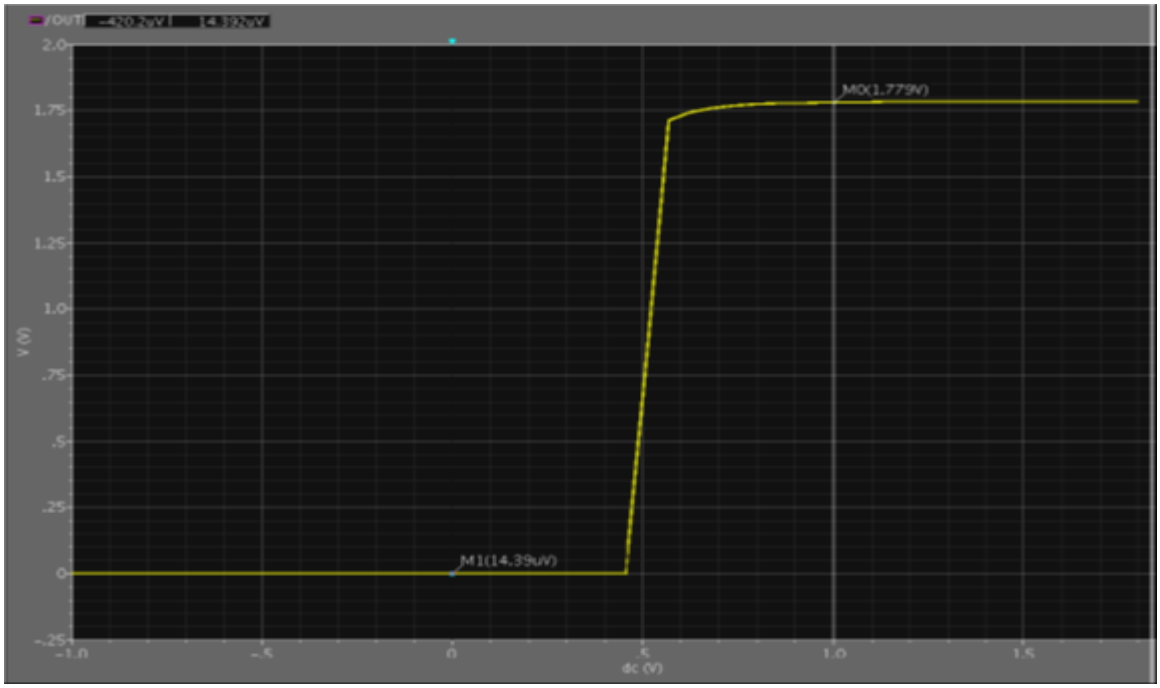

Fig.3 .DC analysis of dynamic comparator wave form

Dynamic comparator transient response

This is often the circuit for shrewd the delay of the Comparator thus for shrewd the delay of the Comparator the Transient Analysis is finished. Here I actually have given input pulse from zero to one.8V to the one input of the Differential combine. And 100mV DC Voltage to the opposite finish of the differential combine. The output wave forms square measure shown in Fig.3.the comparison the input pulse and output wave shape some delay is there. That the average of the 2 ends of the output wave shape as Speed of the Comparator. That the average speed of the Comparator is zero.4618nS.

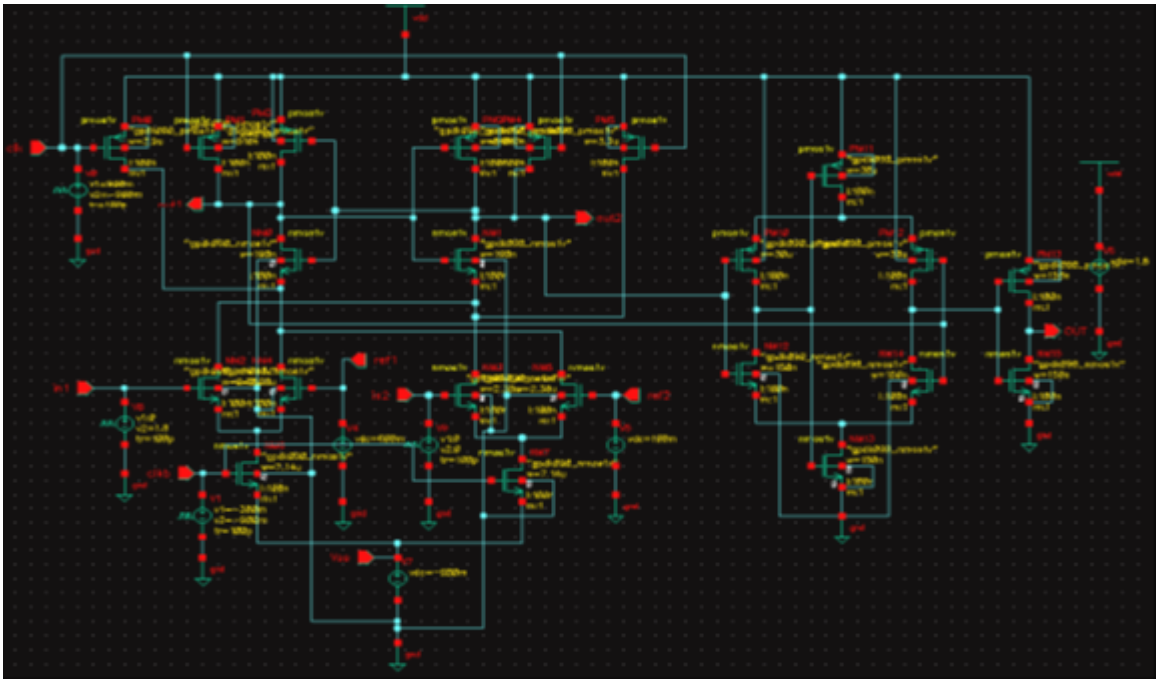

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Fig.3 Dynamic comparator transient response circuit

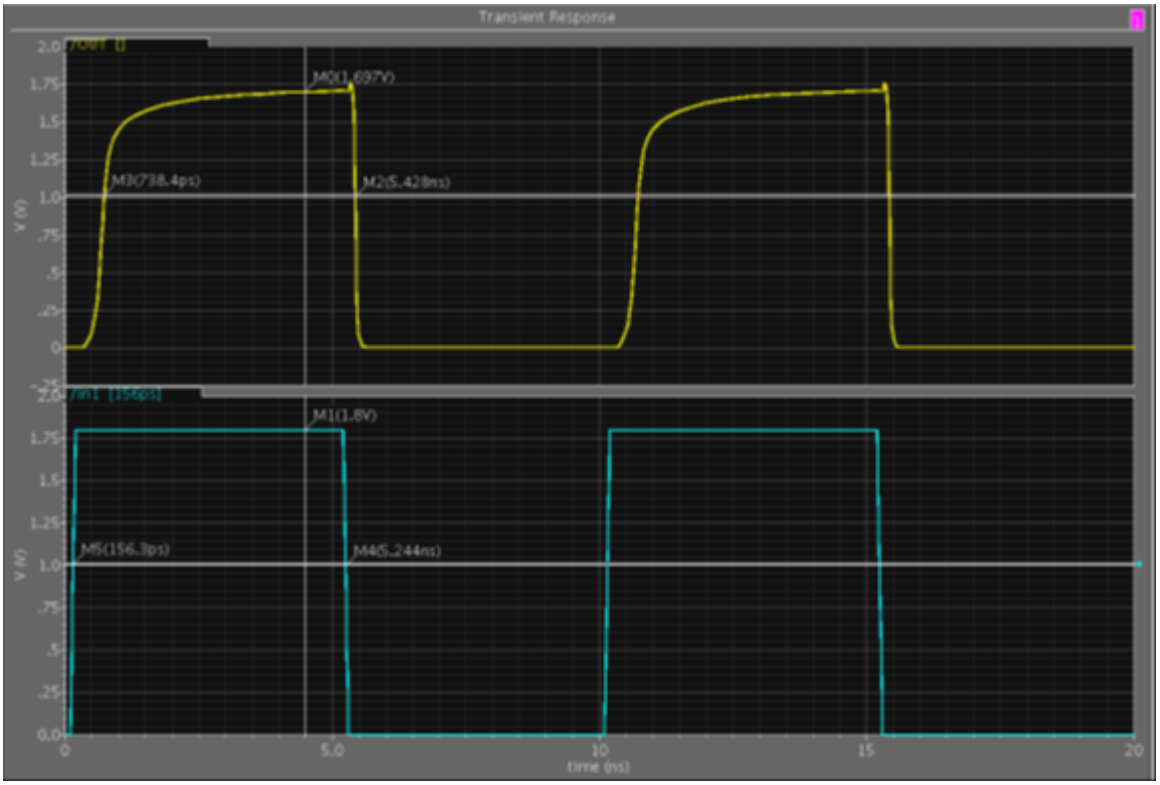

Fig 4 Transient response of dynamic comparator

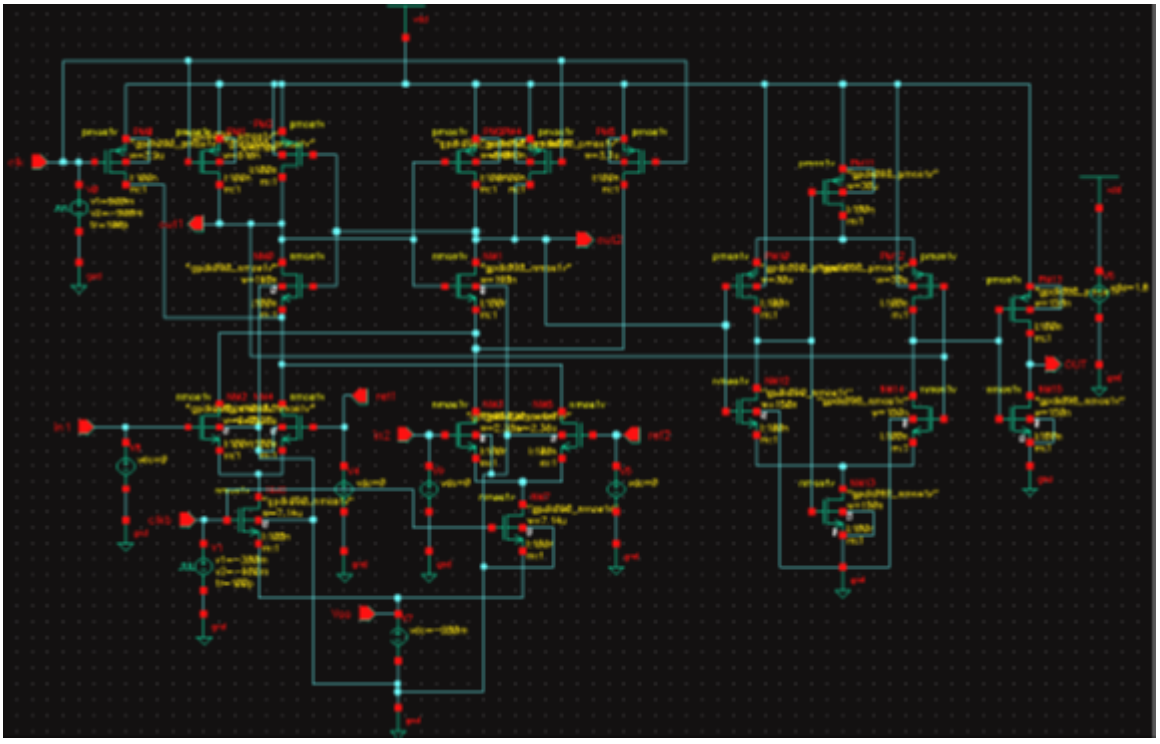

Fig.5.Offset voltage circuit for dynamic comparator

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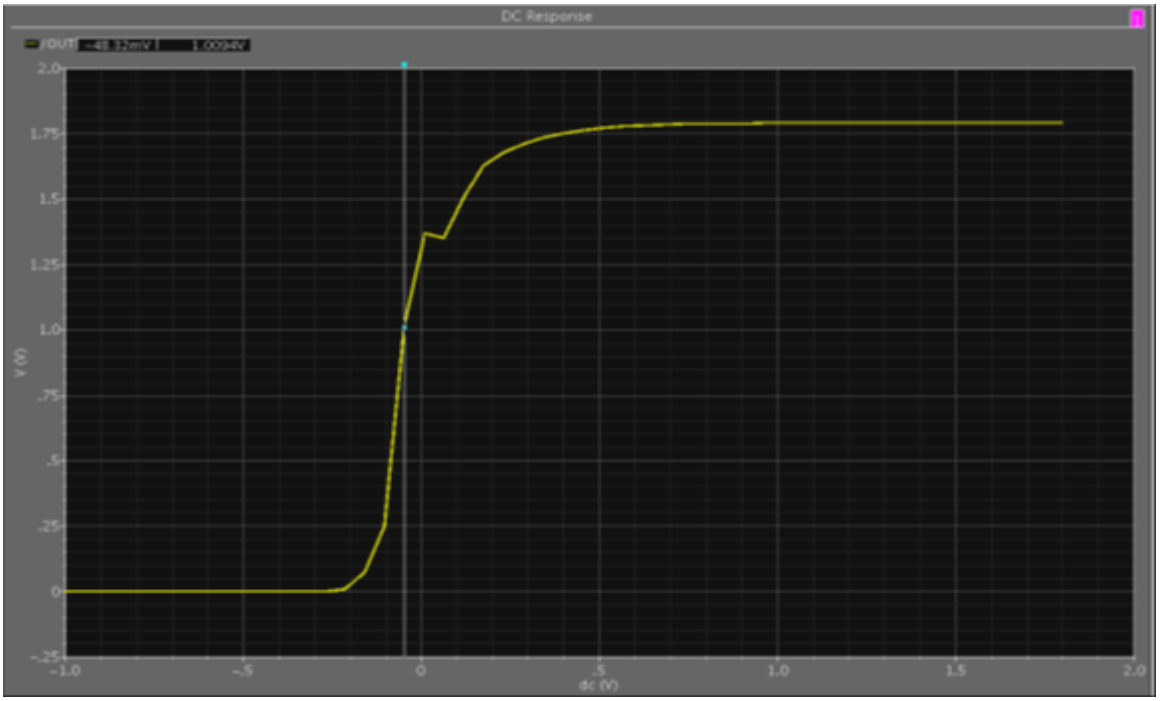

Fig. 6 Offset circuit for dynamic comparator

Summary of Results

Calculation for Delay and speed for Dynamic comparator Vir = 156.3ps Vif = 5.244ns Vor = 738.4ps Vof = 5.428ns Delay = 0.5821ns+0.184ns/2 =0.383ns Speed = 1.83 GHz Power Dissipation= 0.34mw This circuit is the offset of the Dynamic Comparator. Here for finding the offset all the input voltages are given to 0 DC Voltage. The offset waveform is shown in the figure. and calculated offset as 48.32mv. Fig. 6 Offset circuit for dynamic comparator

After post layout simulation calculation for Delay and speed for Dynamic comparator

Vir = 156.3ps Vif = 5.244ns

Vor = 824ps Vof = 5.5ns

Delay = 0.6677ns+0.256 ns/2 =0.4618ns.

Speed = 2.16MHz.

Power Dissipation = 3.543 mw. Area =232.35um2

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