International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue 09
August 2017

Design of Low Delay 32-Bit Parallel Prefix Brentkung Adder

[1]T. Pragna,M.Tech & [2]Mr. K.Ravi,
[1]Scholar, Institute of Aeronautical Engineering, Hyderabad
[2]Assistant Professor, Institute of Aeronautical Engineering, Hyderabad

ABSTRACT -*In VLSI design the excellent performance is produced by a parallel-prefix adder. Nevertheless, the performance can takes large delay through CSLA or CSA. Then, new approachgenerates the Efficiency inBrent-kungAdder. There are two stages of operation in proposed system.They are pre-processing stage and generation stage. The propagate and generate are possessed in the pre-processing stage.Generation stage concentrates on carry generation and final result. Each bit having addition operation in ripple carry adder.Then each bit can wait for the preceding bit addition operation. But the each bit does not wait for preceding bit addition operationin efficient Brent – Kung adder and modification is done at gate level to improve the speed.*

INDEX TERMS: Ripple carry adder, EfficientBrent–Kung adder,Black cell, Gray cell.

I.INTRODUCTION

The Ripple carry adder can perform the addition task. The task is N-bits addition operation will performed by the full adder with N-bits. So, Full adder operation contains sum and carry. That carry is given to the next bit of the full adder operation and this process is continued until the N^{th} bit operation. Hence, the carry of $N\text{-}1^{th}$ bit will be given to the next bit (N) full adder operation in Ripple carry adder.

For Digital Signal Processing and Control Systems the main approach is the addition procedure. The speed and accuracy of the processor or system will depends on the performance of the adder. Multiplexer is a combinational circuit which contains multiple inputs and a single output. The addresses of the addition operation in general purpose processor and DSP processor are abstract from the Ripple carry adder.

The 3-bit ripple carry adder is shown in

Fig.1. The first bit carry is given to second bit full adder and similarly the second bit carry is given to the third bit full adder. In ripple carry adder the addition procedure is performed from least significant bit to most significant bit.

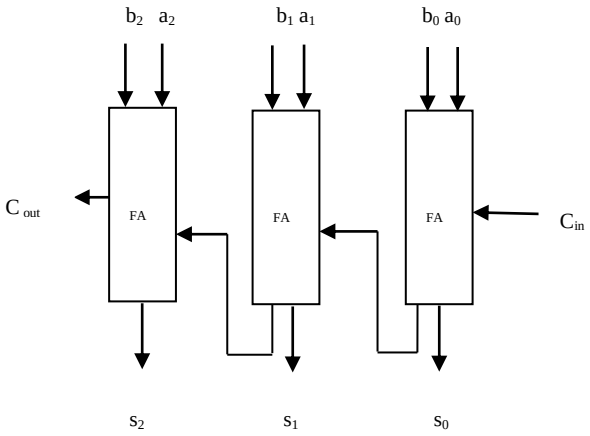

Fig.1: Three Bit Ripple Carry Adder

II. LITERATURE SURVEY

The designing of a Ripple carry adder is simple. However it support more propagation delay (CPD). For reducing the CPD Carry look ahead and carry select (CS)have been proposed. A conventional carry select adder (CSLA) is an RCA-RCA configuration. It produces a pair of sum words and output carry bits corresponding to the carry inputs. A CSLA has less propagation delay compared with the RCA,

but the designing is complex due to its dual RCA configuration. CSLAs of increasing size are connected in series structure in the SQRT CSLA. The main aim of the SQRT CSLA design is to supply a parallel path for carry propagation which helps to reducing the overall adder delay.

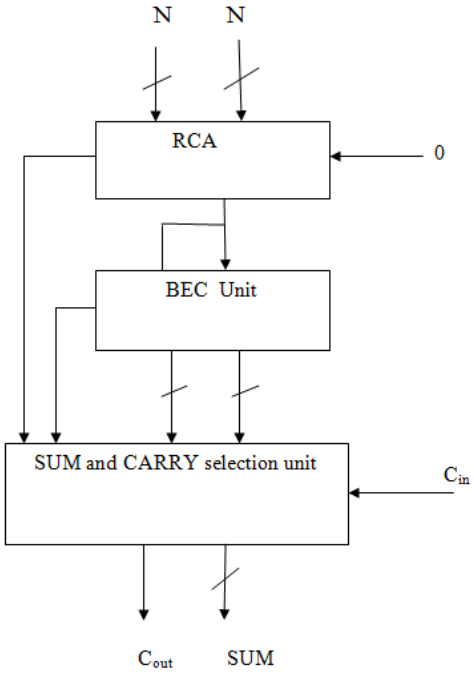

Fig.2: Structure of CSLA

BEC-based CSLA contains binary to excess-l converter which is shown in Fig.2. In the conventional CSLA, The RCA is same as that of BEC. It calculates n-bit sum {so I (i)} and carryout {CO out} corresponds to Cin = O. Inputs to the BEC unit is {soI(i), CO out} and output is (n+ 1).

III.BRENT-KUNG ADDER

For high performance addition operationBrentKung adder is used. It looks like the tree structure for performing the arithmetic operation. Theblack cells and gray cellsare in the Brent-kung adder. Each black cell contains of two AND gates and one OR gate. Each gray cell contains of only one AND gate.Propagate denoted byp_i and it consists of only one AND gate given in equation 1. Generate is denoted by g_i and it consists of one AND gate and OR gate given in equation 2.

$$p_i = A_i \text{ XOR } B_i \text{ ---------- (1)}$$

$$g_i = A_i \text{ AND } B_i \text{ ---------- (2)}$$

Carry generate is denoted by$G_i$and it consists of one AND gate and OR gate given in equation 3 used for first black cell.

$$G_i = p_i \text{ OR } [g_i \text{ AND } c_{in}] \text{ ------ (3)}$$

Now-a-days Field programmable gate arrays [FPGA's] are mostly usedsince they improve the speed of microprocessor based applications like mobile communication, DSP and telecommunication. Development of devices can be done by the research on binary operation fundamentals and motivation. The efficientBrent-kung adder construction contains two stages. They are pre-processing stage and generation stage.

Pre-Processing Stage:

In the pre-processing stage, generate and propagate are obtained from each pair of the inputs. The propagate produce"XOR" operation of input bits and generates gives "AND" operation of input bits. Below equations 4 & 5 shows thepropagate (P_i) and generate (G_i).

$$P_i = A_i \text{ XOR } B_i \text{ ------ (4)}$$

$$G_i = A_i \text{ AND } B_i \text{ ------ (5)}$$

Carry Generation Stage:

In this stage, carry is generated for each bit is called carry generate (C_g) and carry is propagate for each bit is called carry

propagate (C_p). The carry propagate and carry generate are given in below equations 6 & 7.

$$C_p=P_1 \text{ AND } P_0 \text{ ---------- (6)}$$

$$C_g=G_1 \text{ OR } (P_1 \text{ AND } G_0) \text{ ------ (7)}$$

The above C_p and C_g in equations 6&7 is generated in black cell and the below shown carry generation in equation 8 is gray cell. The carry propagate is generated for the further operation. The final cell which is present in the each bit operation gives carry. For the next bit sum operatethis carry is used, the carry generate isgiven in below equations 8.

$$C_g=G_1 \text{ OR } (P_1 \text{ AND } G_0) \text{ ------ (8)}$$

Post-Processing Stage

The carry of a first bit is XORed with the next bit of propagates then the output is given as sum and it is shown in below equation 9.

$$S_i=P_i \text{ XOR } C_{i-1} \text{ ------- (9)}$$

Then, it is used for two thirty-two bit addition operations and each bit experiences the pre-processing stage and generation stage then provides the final sum.

The first input bits move under pre-processing stage and they will produce propagate and generate. Fig.3. shows the step by step process of efficientBrent-kung adder.

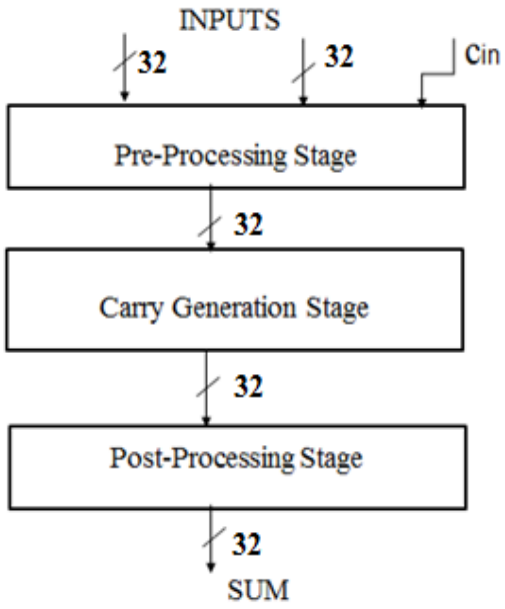

Fig.3: Block Diagram

For the high performance of arithmetic operationsthe efficient Brent-kungadder arrangement is looking like tree structure and it is the high speed adder which focuses on gate level logic. It designs with a reduction of number of gates. So, it decreases the delay and memory used in this architecture.

The efficient Brent-kung adder is shown in fig.4 which improves the speed for the operation of 16-bit addition. The A_i and B_i are the input bits which concentrates on generate and propagate by XOR and AND operations respectively. The propagate and generate undertake the operations of black cell and gray cell and gives the carry C_i. That carry is XORed with the propagate of next bit, which gives us the sum.

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue 09
August 2017

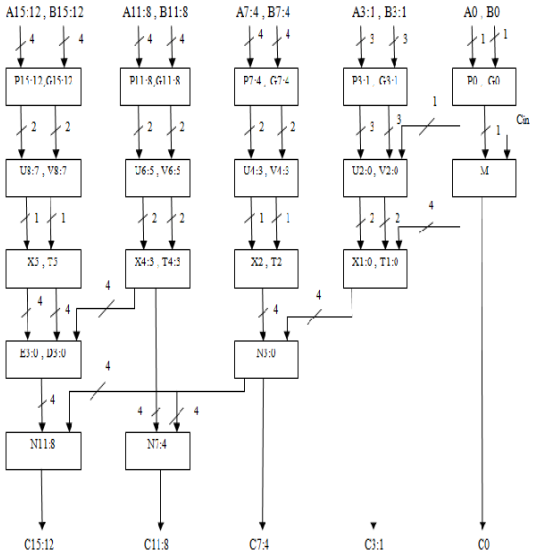

Fig.4: 16-Bit Efficient Brent-kung Adder

The properties of the operations are evaluated in parallel with accept the trees to overlap which leads to parallelization. The architecture ofEfficient Brent-kung adder gives the less delay and less memory for the operation of 16-bit addition.

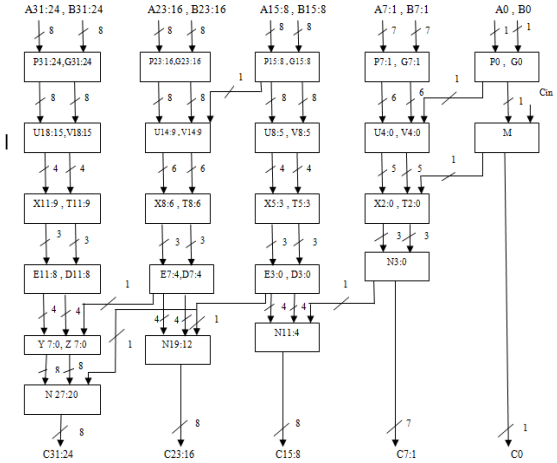

Fig.5: 32-Bit Efficient Brent-Kung Adder

The architecture of 32-bit Efficient Brent-kung adder is shown in Fig.5. The logical circuit is using multiple adders to find the ans i.e., sum of N-bit numbers. Each addition operation has a carry input (C_{in}) which is the previous bit carry output (C_{out}).

Research on binary addition innovatively motivates gives development of devices. Many parallel prefix networks describe the literature of parallel addition operation.The parallel prefix adders are Brent-kung, Kogge-stone, brent-kung, Sklansky, etc,. The fast and accurate performance of an adder gives toused in the very large scale integrated circuits design and digital signal processors.

IV.SIMULATION RESULTS

The Efficient Brent-kung adder is designedin VHDL (very high speed integration hardware description language). Xilinx project navigator 14.1 is used andSimulation results of 32-bit efficient Brent-kungare shown in Fig.6.

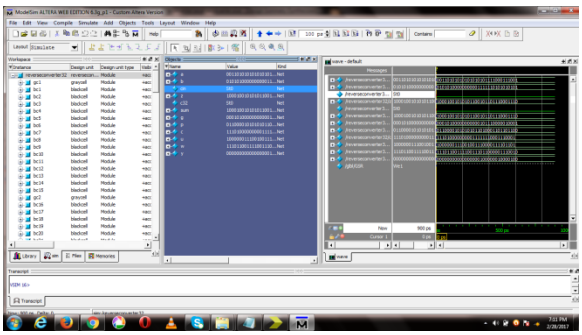

Fig.6: 32-Bit Efficient Brent-kung Adder Simulation Waveform

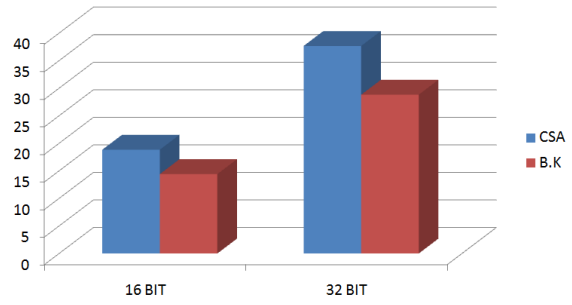

Table.1: Comparison

V.CONCLUSION

In this paper, new approaches are introduced to design an efficient Brent-kung adder look like tree structure. The cells in the carry generation stage are decreased to speed up the binary addition. It focuses on gate levels to perk upthe speed and decreases the memory used.The adder addition operation provideselude great advantage in reducing delay.

VI.REFERENCES

[1] Pakkiraiahchakali, madhukumarpatnala "Designofhigh speed Brent - Kung based carryselectadder" IJSCE march 2013

[2] David h,k hoe, Chris Martinez and srijyothsnavundavalli "Design and characterization of parallel prefix adders using FPGAs", Pages.168-172, march2011 IEEE.

[3] K.Vitoroulis and A.J. Al-Khalili, "performance of parallel prefix adders implemented with FPGA technology," IEEE Northeast Workshop on circuits and systems, pp.498-501, Aug. 2007.

[4] Haridimost.vergos, Member, IEEE and GiorgosDimitrakopoulos, Member, IEEE,"On modulo 2^n+1 adder design"IEEE Trans on computers, vol.61, no.2, feb 2012

[5] GiorgosDimitrakopoulos and DimitrisNikolos, "High-Speed Parallel-Prefix VLSI Ling Adders" IEEE Trans on computers, vol.54, no.2, Feb. 2005.

[6] S.Knowles,"Afamilyofadders," Proc.15th Symp. Comp. Arith.,pp.277-281,June2001.

[7]R.BrentandH.Kung,"Aregularlayoutforparallel adders,"IEEENTrans.Computers,vol. C-31,no.3, pp. 260-264,March1982.

[8] R.E. Brent and M.J. Kung, "Parallel Prefix Computation," J. ACM, vol. 27, no. 4, pages 831-838, Oct. 1980.