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"OVERVIEW ON UPCOMING GENERATION OF MULTI PRUPOSE MICROPROCESSORS"

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ABSTRACT

Our upcoming generation multi-purpose microprocessor (UGMP) is a SPARC V8 (E) based multi-core architecture that provides a significant performance increase compared to earlier generations of European space processors. The presentation will describe the baseline architecture, point out key choices that have been made and will also emphasize points that are still open. The software environments and os that will be available for the UGMP, together with a general overview of the new LEON4 microprocessor, will also be represented

ARCHITECTURAL OVERVIEW

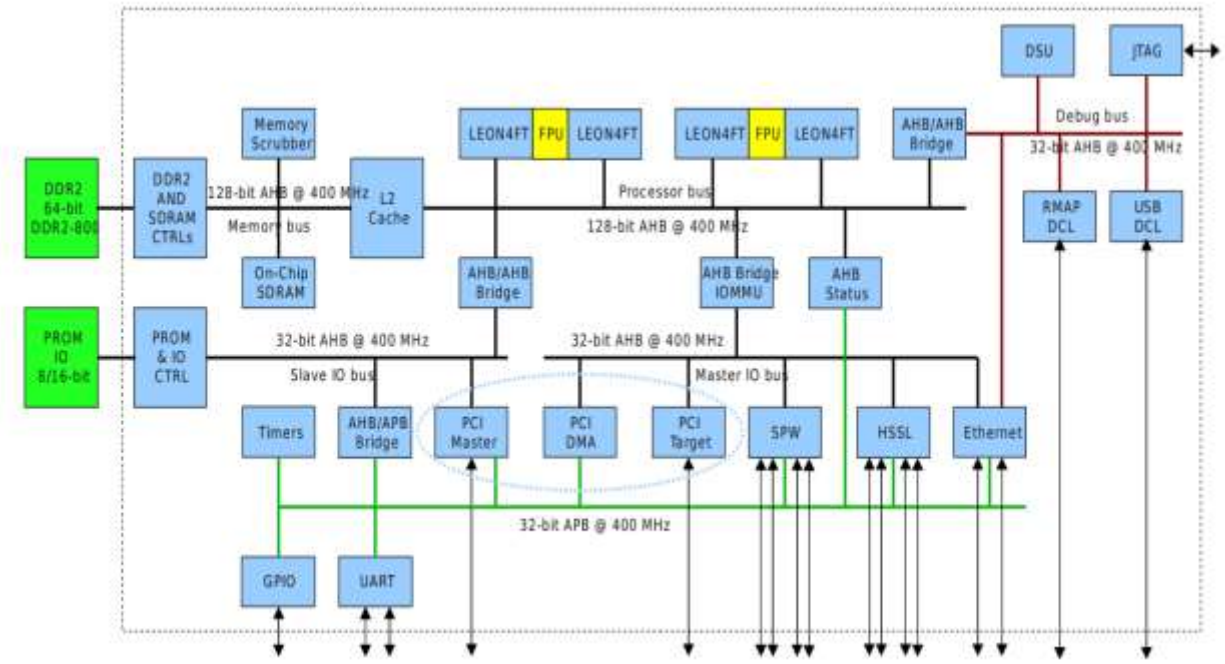

Fig. 1. UGMP Block Diagram

Fig. 1 above depicts an architecture of UGMP. The system will consist of 5 AHB buses, two 32-bit I/O buses, one 128-bit Memory bus and one 32-bit Debug bus. In processor bus there is a LEON4FT cores connected to a shared L2 cache. The bus of memory is located between the L2 cache and the main external memory interfaces, DDR2 and SDRAM interfaces on shared pins, and will include a memory scrubber and possibly on-chip memory. As an alternative to a large on-chip memory, part of the L2 cache could be turned into on-chip memory by cache-way disabling. The I/O bus has been split into two separate buses where all slave interfaces have been placed on one of the buses (Slave I/O bus) and all master interfaces have been placed on the other bus (Master I/O bus). The Master I/O bus connects to the Processor bus via an AHB bridge that provides access restriction (IOMMU) functionality.

The two I/O buses include all peripheral units such as PCI, High-Speed Serial Link, Ethernet MAC, and Space Wire interfaces. The dedicated 32-bit Debug bus connects one debug support unit (DSU), one JTAG debug link, one Space Wire RMAP target, one USB debug communication link, and optionally two Ethernet debug communication links. The Debug bus allows for non-intrusive debugging through the DSU and direct access to the complete system, since the Debug bus is not placed behind an AHB bridge with access restriction functionality.

All I/O master units in the system contain dedicated DMA engines and are controlled by descriptors located in main memory that are set up by the processors. Reception of, for instance, Ethernet and SpaceWire packets will not increase CPU load. The cores will buffer incoming packets and write them to main memory without processor intervention.

The target frequency of the LEON4FT and on-chip buses is 400 MHz, but depends ultimately on the implementation technology. The SDRAM interface will be able to run at the same or one third of the system frequency. The DDR2 interface will be run at the same or twice the system frequency. The clock scaling factor between the memory interfaces and the rest of the chip is selectable via an external signal.

SYSTEM ARCHITECTURE

- *128-bit Processor AHB bus*
  - *4x LEON4FT with 16 + 16 KiB cache, SPARC Reference MMU, physical snooping, 32-bit MUL/DIV and GRFPU shared between pairs of LEON4FT with 4-word instruction FIFO, or*
  - *(TBD) dedicated GRFPU for each processor core.*
  - *1x Shared L2 cache with memory access protection (fence registers)*
  - *1x 128-bit to 32-bit unidirectional AHB to AHB Bridge (connecting Debug bus with Processor Bus)*
  - *1x 128-bit to 32-bit unidirectional AHB to AHB Bridge (connecting Processor bus to slave IO Bus)*
  - *1x 32-bit to 128-bit unidirectional AHB to AHB Bridge with IOMMU (connecting master IO bus To Processor bus)*
- *128-bit Memory AHB bus*
  - *1x 64-bit DDR2-800 memory interface with Reed-Solomon ECC (16 or 32 check bits)*
  - *1x 64-bit SDRAM PC133 memory interface with Reed-Solomon ECC (16 or 32 check bits)*
  - *1x Memory scrubber*
  - *1x On-chip SDRAM (if available on the target technology)*
- *32-bit Master I/O AHB bus*
  - *4x SpaceWire cores with redundant link drivers and RMAP @ 200 Mbit/s*
  - *4x High-Speed Serial Link with SpaceFibre interface, if IP's available*
  - *2x 10/100/1000 Mbit Ethernet interface with MII/GMII PHY interface*
  - *1x 32-bit PCI target interface @ 66 MHz*
- *32-bit Slave I/O AHB bus*
  - *1x 32-bit PCI master interface @ 66 MHz with DMA controller mapped to the Master I/O bus*
  - *1x 8/16-bit PROM/IO controller with BCH ECC*
  - *1x 32-bit AHB to APB bridge, connecting 32-bit APB bus:*
    - *1x General purpose timer unit*
    - *1x 16-bit general purpose I/O port controller*
    - *2x 8-bit UART interface*
    - *1x Multiprocessor interrupt controller*
    - *4x Secondary interrupt controller*
    - *1x PCI arbiter with support for four agents*
    - *1x AHB status register*
    - *1x General Purpose register for clock gating*
- *32-bit Debug AHB Bus*
  - *1x Debug support unit*
  - *1x USB debug link*
  - *1x JTAG debug link*
  - *1x SpaceWire RMAP target*

LEON4 MICROPROCESSOR AND L2 CACHE

It is the latest processor in the LEON series. LEON$ is a 32-bit processor core conforming to the SPARC

V architecture. It is basically designed for embedded applications, combining high performance with low complexity and low power consumption.*
The improvements includes:

- *Branch Prediction*
- *64-bit pipeline with single cycle load/store*
- *128-bit wide L1 cache*
- *4-port register file*

An important factor to high processor performance and good SMP scaling is high memory bandwidth coupled with low latency. A 128-bit AHB bus will therefore be used to connect the LEON4FT processors. This will allow 32 bytes to be read in 2 clocks, not counting the initial memory latency. To mask memory latency, the GRLIB L2 cache will be used as a high-speed buffer between the external memory and the AHB bus. A read hit to the L2 cache typically requires 3 clocks, while a write takes 1 clock. A 32-byte cache line fetch will be performed as a burst of two 128-bit reads. The first read will have a delay of 3 clocks and the second word will be delivered after one additional clock. A cache line will thus be fetched in 4 clocks (3 + 1). Error correction will add an additional latency of 1 clock to all read accesses to allow time for checksum calculation.

IMPROVEMENT IN MULTI-PROCESSOR OPERATION

Beyond support for standard SMP configurations, e.g. with a central multi-processor interrupt controller, UGMP will also support ASMP configurations: Per CPU-core dedicated timer units and interrupt controllers allow running separate operating systems on each of the cores. In addition to the MMU's in each of the CPU cores and the IOMMU, memory read/write access protection (fence registers) implemented in the L2 cache also improves the time and space partitioning.

INSTRUCTION SET

Beyond support for standard SMP configurations, e.g. with a central multi-processor interrupt controller, UGMP will also support ASMP configurations: Per CPU-core dedicated timer units and interrupt controllers allow running separate operating systems on each of the cores. In addition to the MMU's in each of the CPU cores and the IOMMU, memory read/write access protection (fence registers) implemented in the L2 cache also improves the time and space partitioning.

The overall accuracy will depend on the accuracy of the simulation models for the DDR2 memory controller and the L2 cache. The target is 10 % which is considered challenging but will be the goal during the development.

SOFTWARE SUPPORT

The GRMON debug monitor from Aeroflex Gaisler will be extended to support all new functionality for debugging and profiling that will be included in the UGMP. The hardware platform will provide full backwards compatibility with existing LEON3FT software and all standard compilers that can produce correct SPARC V8 code can be used.

Board support packages for the UGMP will be delivered for the following operating systems:

- *RTEMS 4.8 and 4.10*
- *eCos*
- *VxWorks 6.7*
- *Linux 2.6*

CONCLUSION

UGMP will be a SPARC V8 (E) based multicore architecture that provides brilliantly performance increase compared to earlier generations of European space processors, with high-speed interfaces such as SpaceWire and Gigabit Ethernet on-chip. The platform will have improved support for profiling and debugging compared to previous generations of European space processors and will have a rich set of software immediately available due to backwards compatibility with existing SPARC V8 software and LEON3 board support packages.

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