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Implementation of Low Power Programmable Prpg With Test Compression Capabilities

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ABSTRACT:

This paper describes a low power(LP) programmable generator capable of producing pseudorandom test patterns with desired toggling levels and improved blame scope slope contrasted with the best with date worked in built in self test (BIST) based pseudorandom test design generators. It is included a direct limited state machine driving a fitting stage shifter, and it accompanies various components enabling this gadget to deliver paired successions with preselected toggling (PRESTO) action. We acquaint a strategy with naturally select a few controls of the generator offering simple and exact tuning. A similar method is in this way utilized to deterministically control the generator toward test arrangements with enhanced blame scope to design tally proportions. Besides, this paper proposes a LP test pressure technique that permits molding the test control envelope in a completely unsurprising, precise, and adaptable design by adjusting the PRESTO based rationale BIST (LBIST) frame work. The proposed mixture plot effectively consolidates test pressure with LBIST, where the two systems can work synergistically to convey top notch tests. Exploratory outcomes got for mechanical outlines represent the attainability of the proposed test plots and are accounted for thus.

Key Words-Built in self test (BIST), low power (LP) test, pseudorandom test pattern generators (PRPGs), test data volume compression.

I. INTRODUCTION

Although the following years, the essential goal of assembling test will remain basically the same to guarantee dependable and astounding semiconductor items conditions and thusly additionally test arrangements may experience a critical advancement. The semiconductor innovation, outline qualities, and the plan procedure are among the key factors that will affect this development. With new sorts of imperfections that one should consider to give the coveted test quality to the following innovation hubs, for example, 3-D, it is appropriate to suggest the conversation starter of what coordinating plan for test (DFT) strategies should be conveyed. Test pressure, presented 10 years prior, has rapidly turned into the standard DFT strategy. In any case, it is indistinct whether test compression will be fit for adapting to the quick rate of mechanical changes throughout the following decade. Strangely, rationale worked in individual test (LBIST), initially created for logic built in self test and in-field test, is presently picking up acknowledgment for generation test as it gives extremely hearty DFT and is utilized progressively frequently with test pressure. This half and half approach is by all accounts the following sensible developmental stride in DFT. It has potential for enhanced test quality; it might expand the capacities to keep running at speed control mindful tests, and it can lessen the cost of assembling test while protecting all LBIST and output pressure points of interest.

Attempts to conquer the bottleneck of test information transmission capacity between the analyzer and the chip have made the idea of consolidating LBIST and test information pressure an imperative innovative work territory. Likewise with traditional output based test, half and half plans, because of the high information action related with examine based test operations, may expend substantially more power than a circuit-under-test was intended to work under. With overemphasizing gadgets past the mission mode, diminishments in the working

energy of ICs in a test mode have been of worry for a considerable length of time. Full flip sweep examples may draw a few times the normal useful mode power, and this pattern keeps on developing, especially finished the mission mode's pinnacle control. This power prompted over test may bring about warm issues, voltage commotion, control hang, or intemperate pinnacle control over different cycles which, thusly, cause a yield misfortune because of moment gadget harm, extreme lessening in chip unwavering quality, shorter item lifetime.

II. LITERATURE SURVEY

1)A. Hertwig and H.-J. Wunderlich presents a new pseudorandom test pattern generator with preselected toggling (PRESTO) activity. It is comprised of a linear finite state machine (a linear feed backshift register or a ring generator) driving an appropriate phase shifter and armed with a number of features that allows this device to produce binary sequences with low toggling (switching) rates while preserving test coverage achievable by the best to date conventional BIST-based PRPGs with negligible impact on test application time.

2) N. A. Touba and E. J. McCluskey presents a low transition test pattern generator, called LT-LFSR, to reduce average and peak power of a circuit during test by reducing the transitions within randomtest pattern and between consecutive patterns. In other words, transitions are reduced in two dimensions, i.e. between consecutive patterns and bits. LT-LFSR is independent of circuit under test and flexible to be used for both BIST and scan-based BIST architectures.The experimental results for ISCAS'85 and '89 bench marks, confirm up to 77% and 49% reduction in average and peak power, respectively. Power consumption of digital systems may increase significantly during testing.

3) M. Nourani, M. Tehranipoor Presents a Power consumption of digital systems may increase significantly during testing. In this paper, systems equipped with a scan-based built-in self-test like the STUMPS architecture are analyzed, the modules and modes with the highest power consumption are identified, and design modifications to reduce power consumption are proposed. The design modifications include some gating logic for masking the scan path activity during shifting, and the synthesis of additional logic for suppressing random patterns which do not contribute to increase the fault coverage. These design changes reduce power consumption during BIST by several orders of magnitude, at very low cost in terms of area and performance. Independently, self test techniques have been developed which can be classified into "test-per-clock" schemes and "test-per-scan" schemes.

4) D.Das and N.A.Touba Presents a new lossless test vector compression scheme is presented which combines linear feedback shift register(LFSR) reseeding and statistical coding in a powerful way. Test vectors can be encoded as LFSR seeds by solving a system of linear equations. The solution space of the linear equations can be quite large. The proposed method takes advantage of this large solution space to find seeds that can be efficiently encoded using a statistical code. Two architectures for implementing LFSR reseeding with seed compression are described. One configures the scan cells themselves to perform the LFSR functionality while the other uses a new idea of "scan windows" to allow the use of a small separate LFSR whose size is independent of the number of scan cells. The proposed scheme can be used either for applying a fully deterministic test set or for mixed-mode built in self test(BIST), and it can be used in conjunction with other variations of LFSR reseeding that have been previously proposed to further improve the encoding efficiency.

III. EXISTING SYSTEM

1. Presto Generator

The essential structure of a PRESTO generator. A n-bit PRPG associated with a stage shifter bolstering examine chains shapes a portion of the generator creating the genuine pseudorandom test designs. A straight criticism move enroll or a ring generator can execute a PRPG. All the more significantly, in any case, n hold hooks are put between the PRPG and the stage shifter. Each hold lock is independently

controlled through a relating phase of a n-bit flip control enroll. For whatever length of time that its empower input is declared, the given lock is straightforward for information going from the PRPG to the stage shifter, and it is said to be in the flip mode. At the point when the hook is impaired, it catches and spares, for various clock cycles, the comparing bit of PRPG, subsequently encouraging the stage shifter (and perhaps some sweep chains) with a consistent esteem. It is currently in the hold mode. It is important that each stage shifter yield is acquired by XOR yields of three distinctive hold hooks. In this way, every sweep chain stays in a low control mode gave just incapacitated hold hooks drive the comparing stage shifter yield .

As specified already, the flip control enlist super tight clamps the hold hooks. Its substance includes 1s, where 1s show locks in the flip mode, in this way straightforward for information touching base from the PRPG. Their division decides an output exchanging action. The control enlist is reloaded once per design with the substance of an extra move enroll. The empower signals infused into the move enlist are created in a probabilistic manner by utilizing the first PRPG with a programmable arrangement of weights. The weights are dictated by four AND entryways delivering 1s with the likelihood of 0.5, 0.25, 0.125, and 0.0625, individually. The OR entryway permits picking probabilities past straightforward forces of 2. A 4-bit enlist Switching is utilized to initiate AND doors, and permits choosing a client characterized level of exchanging movement. For instance, the exchanging code 0100 will set to 1, on the normal, 25% of the control enlist stages, and in this manner 25% of hold hooks will be empowered. Given the stage shifter structure, one can survey then the measure of output chains getting steady esteems, and along these lines the normal flipping proportion. An extra 4-input NOR door recognizes the exchanging code 0000, which is utilized to turn the LP usefulness off. It is important that when working in the weighted arbitrary mode, the exchanging level selector guarantees factually stable substance of the control enlist as far as the measure of 1s it conveys. Therefore, generally a similar portion of output chains will remain in the LP mode, however an arrangement of genuine low flipping chains will continue changing starting with one test design then onto the next. It will relate to a specific level of flipping in the output chains. With just 15 distinctive exchanging codes, be that as it may, the accessible flipping granularity may render this arrangement excessively coarse, making it impossible to be constantly worthy. Area introduces extra components that make the PRESTO generator completely operational in an extensive variety of wanted exchanging rates.

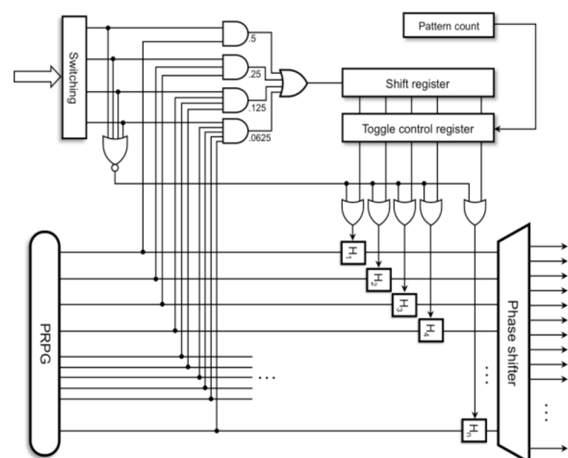

Fig1a) Basic architecture of presto Generator.

III. PROPOSED SYSTEM

Considerably higher adaptability in shaping low flipping test examples can be accomplished by conveying a plan introduced in Fig. 2. Basically, while protecting the operational standards of the fundamental arrangement, this approach parts up a moving time of each test design into a succession of substituting hold and flip interims. To move the generator forward and backward between these two states, we utilize a T sort flip slump that switches at whatever point there is a 1 on its information input. On the off chance that it is set to 0, the generator enters the hold time frame with all locks incidentally incapacitated paying little mind to the control enroll content. This is proficient by setting AND doors on the control enroll yields to permit solidifying of all stage shifter inputs. This property can be significant in SOC plans where just a solitary output chain crosses a given center, and its anomalous

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flipping may cause locally inadmissible warmth scattering that must be lessened because of transitory hold periods. On the off chance that the T flip tumble is set to 1 (the flip time frame), at that point the locks empowered through the control enlist can finish test information moving from the PRPG to the sweep chains.

Two extra parameters kept in 4-bit Hold and Toggle registers decide to what extent the whole generator remains either in the hold mode or in the flip mode, separately. To end either mode, a 1 must happen on the T flip tumble input. This weighted pseudorandom flag is delivered in a way like that of weighted rationale used to nourish the move enroll. The T flip slump controls additionally four 2-input multiplexers steering information from the Toggle and Hold registers. It permits choosing a wellspring of control information that will be utilized as a part of the following cycle to perhaps change the operational method of the generator. For instance, when in the flip mode, the information multiplexers watch the Toggle enroll. Once the weighted rationale yields 1, the flip-tumble flips, and thus all hold locks solidify in the last recorded state. They will stay in this state until the point when another 1 happens on the weighted rationale yield. The irregular event of this occasion is presently identified with the substance of the Hold enroll, which decides when to end the hold mode. A sweep exchanging profile while conveying the PRESTO generator in a theoretical domain with 15 filter chains.

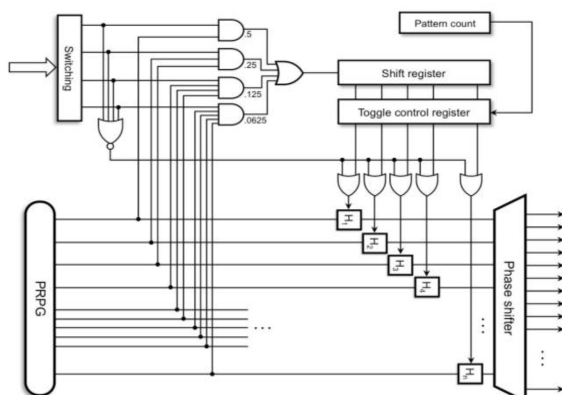
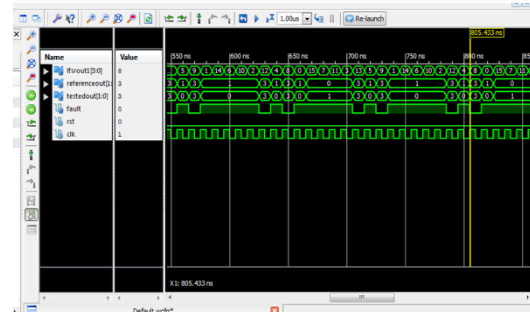


Fig1b): Fully Operation Version of PRESTO

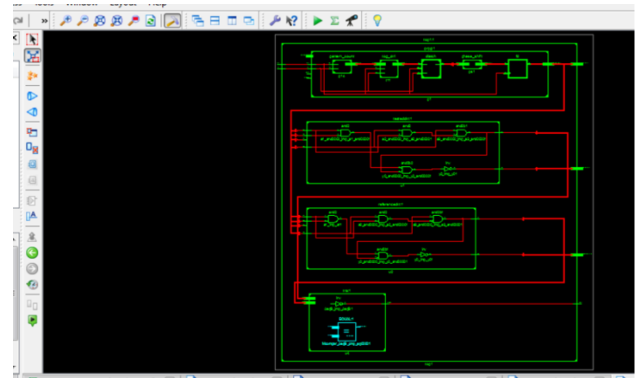
V. RESULTS

Simulation Result:



Synthesis Results:

RTL Schematic:



VI. CONCLUSION

The proposed approach show the concept of reducing the transitions in the test pattern generated. The transition is reduced by increasing the correlation between the successive bits. The simulation results shows that how the patterns are generated for the applied seed vector. This paper presents the implementation with regard to verilog language. Synthesizing and implementation of the code is carried out on Xilinx Project Navigator, ISE 8.2i suite. The power reports shows that the proposed low power lfsr consumes less power during testing by taking the benchmark circuit C17 . In future there is a chance to reduce the power somewhat more by doing modifications in the proposed architecture.

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