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Three-Phase Multilevel Inverter With Reduced Number of Power Electronic Components

Chennaiah Banoth[1], Mahender kodela [2], Kumaraswamy Madavena[3]

[1] *Assistant Professor Department of Facilities and Services Planning (Building Technology and services),Jawaharlal Nehru Architecture and Fine Arts University, Hyderabad, Telangana, India*

[2] *Assistant Professor Department of Electrical and Electronics Engineering,* Vaagdevi College Of Engineering, warangal, Telangana, India.

[3] *Associate Professor Department of Electrical and Electronics Engineering,* Ganapthi Engineering College, warangal, Telangana, India.

banoth.chennaiah@gmail.com & mahi.kodela@gmail.com & kumar21sriram@gmail.com

Abstract—*In this paper, a new configuration of a three-phase five-level multilevel voltage-source inverter is introduced. The proposed topology constitutes the conventional three-phase two-level bridge with three bidirectional switches. Multilevel inverters are mainly used in medium voltage and high power applications to reduce the required voltage rating of the power semiconductor switching devices. On the other hands, these multilevel inverters are attractive for various applications regardless of the power ratings because they can essentially realize lower harmonics with lower switching frequency and lower electromagnetic interference (EMI). In this context, the multilevel inverters with larger number of levels suitable for circuit integration are actively investigated. A multilevel dc link usin fixed dc voltage supply and cascaded half-bridge is connected I such a way that the proposed inverter outputs the required output voltage levels. The fundamental frequency staircase modulation technique is easily used to generate the appropriate switching gat signals. For the purpose of increasing the number of voltage level with fewer number of power electronic components, the structure of the proposed inverter is extended and different methods to determine the magnitudes of utilized dc voltage supplies are suggested Moreover, the prototype of the suggested configuration is manufactured as the obtained simulation and hardware results ensure the feasibility of the configuration and the compatibility of the modulation technique is accurately noted.*

Keywords— Multilevel inverters, voltage balancing circuit, boost function, Diode-Clamped Inverter

I. INTRODUCTION

Require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. The concept of multilevel converters has been introduced since 1975 [4]. The term multilevel began with the three-level converter [5]. Subsequently, several multilevel converter topologies have been developed [6-13]. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows. ● Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced. ● Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced.

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Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [14]. ● Input current: Multilevel converters can draw input current with low distortion. ● Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

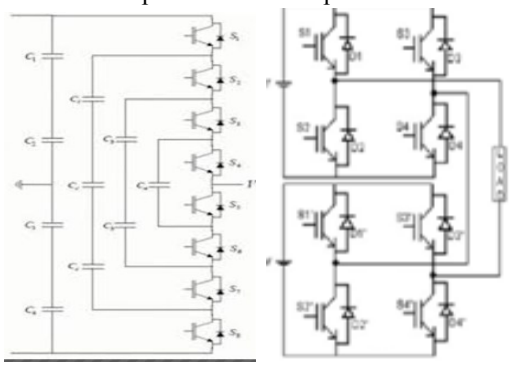

Fig.1 Typical Circuit Topologies of Multilevel Inverters.

Fig. 1(a) and (b) shows the typical configuration of the proposed three-phase five-level multilevel inverter. Three bidirectional switches (S1–S6, Da1–Dc2), two switches–two diodes type, are added to the conventional three-phase two-level bridge (Q1–Q6). The function of these bidirectional switches is to block the higher voltage and ease current flow to and from the midpoint (o). A multilevel dc link built by a single dc voltage supply with fixed magnitude of 4Vdcand CHB having two unequal dc voltage supplies of Vdc and 2Vdc are connected to (+,–,o) bridge terminals. Based on the desired number of output voltage levels, a number of CHB cells are used. Since the proposed inverter is designed to achieve five voltage levels, the power circuit of the CHB makes use of two series cells having two unequal dc voltage supplies. In each cell, the two switches are turned ON and OFF under inverted conditions to output two different voltage levels.

The first cell dc voltage supply Vdc is added if switch T1 is turned ON leading to Vmg=+Vdc where Vmg is the voltage at node (m)with respect to inverter ground (g)or bypassed if switch T2 is turned ON leading to Vmg=0. Likewise, the second cell dc voltage supply 2Vdc is added when switch T3 is turned ON resulting in Vom=+2VdcwhereVomis the voltage at midpoint(o)with respect to node(m)or by passed when switch T4 is turned ON resulting in Vom =0.The peak voltage rating of the switches of the conventional two level bridge (Q1–Q6) is 4Vdcwhereas the bidirectional switches(S1–S6) have a peak voltage rating of 3Vdc.InCHBcells,thepeak voltage rating of second cell switches (T3 and T4) is 2Vdcwhile the peak voltage rating of T1 and T2 in the first cell is Vdc. By considering phase, the operating status of the switches and the inverter line-to-ground voltage Vag are given in Table I.

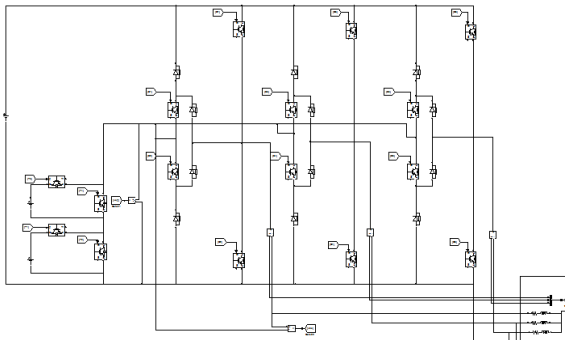

Fig. 1. Circuit diagram of the proposed three-phase five-level multilevel inverter

TABLE I

Switching State Sa and Inverter Line-to-Ground Voltage Va

Sa	Q1	S1	S2	Q2	T1	T2	T3	T4	Vag
4	on	off	off	off	on	off	on	off	+4Vdc
3	off	on	on	off	on	off	on	off	+3Vdc
2	off	on	on	off	off	on	on	off	+2Vdc
1	off	on	on	off	on	off	off	on	+Vdc
0	off	off	off	on	on	off	off	on	0

Proposed topology:

Fig. 1(a) and (b) shows the typical configuration of the proposed three-phase five-level multilevel inverter. Three bidirectional switches (S1–S6, Da1–Dc2), two switches–two diodes type, are

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added to the conventional three-phase two-level bridge (Q1–Q6). The function of these bidirectional switches is to block the higher voltage and ease current flow to and from the midpoint (o). A multilevel dc link built by a single dc voltage supply with fixed magnitude of 4Vdcand CHB having two unequal dc voltage supplies of Vdc and 2Vdc are connected to (+,–,o) bridge terminals. Based on the desired number of output voltage levels, a number of CHB cells are used. Since the proposed inverter is designed to achieve five voltage levels, the power circuit of the CHB makes use of two series cells having two unequal dc voltage supplies. In each cell, the two switches are turned ON and OFF under inverted conditions to output two different voltage levels.

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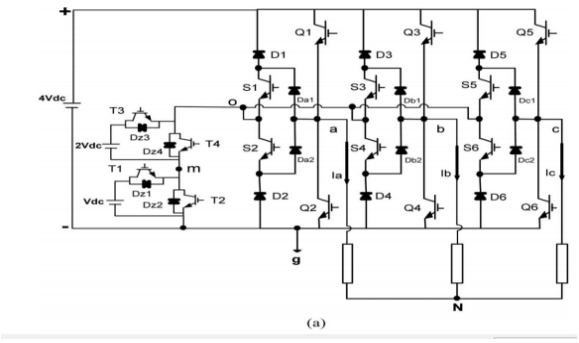

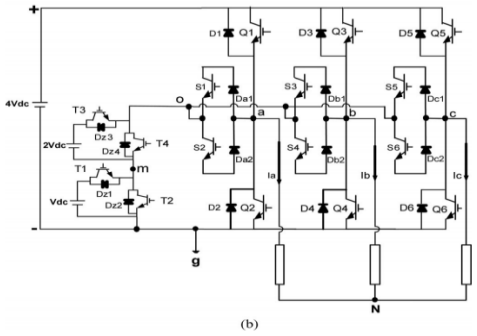

Fig. 1. Circuit diagram of the proposed three-phase five-level multilevel inverter

TABLE I

Switching State Sa and Inverter Line-to-Ground Voltage Va

Sa	Q1	S1	S2	Q2	T1	T2	T3	T4	Vag
4	on	off	off	off	on	off	on	off	+4Vdc
3	off	on	on	off	on	off	on	off	+3Vdc
2	off	on	on	off	off	on	on	off	+2Vdc
1	off	on	on	off	on	off	off	on	+Vdc
0	off	off	off	on	on	off	off	on	0

It is easier to define the inverter line-to-ground voltages Vag, Vbg, and Vcg in terms of switching states Sa, Sb, and Scas

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = \frac{4V_{dc}}{N-1} * \begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} \quad (1)$$

Where N=5 is the maximum number of voltage levels. The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table II. The inverter may have 24 different modes within a cycle of the output waveform. According to Table II, it can be noticed that the bidirectional switches operate in 18 modes. For each mode, there is no more than one bidirectional switch in on state. As a result, the load current commutates over one switch and one diode (for instance: in (410), the load current Ib can flow in

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S3 and Db1 or S4 and Db2). Since some insulated gate bipolar transistors (IGBTs) share the same switching gate signals, the proposed configuration significantly contributed in reducing the utilized gate driver circuits and system complexity. The inverter line-to-line voltage waveforms Vab, Vbc, and Vca with corresponding switching gate signals are depicted in Fig. 2whereVab,Vbc, and Vca are related to Vag, Vbg, and Vcg.

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix}. \quad (2)$$

The inverter line-to-neutral voltages VaN, VbN, and VcN may be expressed as

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix}. \quad (3)$$

It is useful to recognize that the inverter voltages at terminals a, b, and c with respect to

the id point(o)are given by

$$\begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} = \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} - \begin{bmatrix} V_{og} \\ V_{og} \\ V_{og} \end{bmatrix} \quad (4)$$

whereVogis the voltage at midpoint(o)with respect to groun (g). Vogroutinely fluctuates among three different voltage valuesVdc,2Vdc, and 3Vdcas follows

$$V_{og} = \begin{cases} V_{dc}, & \text{if } Sa + Sb + Sc \leq 5 \\ 2V_{dc}, & \text{if } Sa + Sb + Sc = 6 \\ 3V_{dc}, & \text{if } Sa + Sb + Sc \geq 7. \end{cases} \quad (5)$$

The simulated voltage waveforms ofVag,Vog,Vao, and VaN based on (1)–(5) are shown in Fig. 3 where, for instance, 13 sequent voltage steps are seen in VaN waveform as follows +8Vdc/3, +7Vdc/3, +6Vdc/3, +5Vdc/3, +4Vdc/3, +2Vdc/3, 0 –2Vdc/3, –4Vdc/3, –5Vdc/3, –6Vdc/3,–7Vdc/3, and –8Vdc/3 It is worth noting that all simulated waveforms are obtained a t1=t2 =···=t24=0.02/24 s. In order to plot the space vecto diagram of the proposed inverter in a stationaryd–qreferenc frame, the following equations can be used to derive dandqvoltage components for all inverter vectors: TABLE I I

Switching states sequence of the proposed inverter with in one cycle

Switches	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	S_1	S_2	S_3	S_4	S_5	S_6	T_1	T_2	T_3	T_4
t_1	1	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1
t_2	1	0	0	0	0	1	0	0	1	1	0	0	1	0	0	1
t_3	1	0	0	0	0	1	0	0	1	1	0	0	0	1	1	0
t_4	1	0	0	0	0	1	0	0	1	1	0	0	1	0	1	0
t_5	1	0	1	0	0	1	0	0	0	0	0	0	1	0	1	0
t_6	0	0	1	0	0	1	1	1	0	0	0	0	1	0	1	0
t_7	0	0	1	0	0	1	1	1	0	0	0	0	0	1	1	0
t_8	0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	1
t_9	0	1	1	0	0	1	0	0	0	0	0	0	1	0	0	1
t_{10}	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	1
t_{11}	0	1	1	0	0	0	0	0	0	0	1	1	0	1	1	0
t_{12}	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1	0
t_{13}	0	1	1	0	1	0	0	0	0	0	0	0	1	0	1	0
t_{14}	0	1	0	0	1	0	0	0	1	1	0	0	1	0	1	0
t_{15}	0	1	0	0	1	0	0	0	1	1	0	0	0	1	1	0
t_{16}	0	1	0	0	1	0	0	0	1	1	0	0	1	0	0	1
t_{17}	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1
t_{18}	0	0	0	1	1	0	1	1	0	0	0	0	1	0	0	1
t_{19}	0	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0
t_{20}	0	0	0	1	1	0	1	1	0	0	0	0	1	0	1	0
t_{21}	1	0	0	1	1	0	0	0	0	0	0	0	1	0	1	0
t_{22}	1	0	0	1	0	0	0	0	0	0	1	1	1	0	1	0
t_{23}	1	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0
t_{24}	1	0	0	1	0	0	0	0	0	0	1	1	1	0	0	1

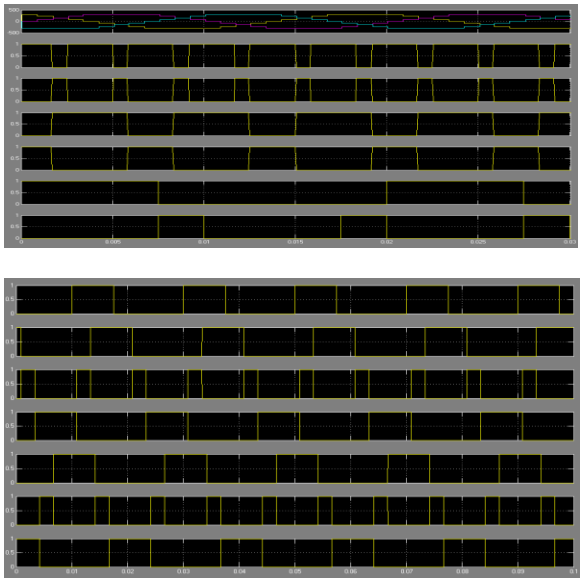

Fig. 2. Simulated waveforms ofVab,Vbc,andVca with corresponding switching gate signals fo the proposed inverter at fundamental frequency f=50 Hz.

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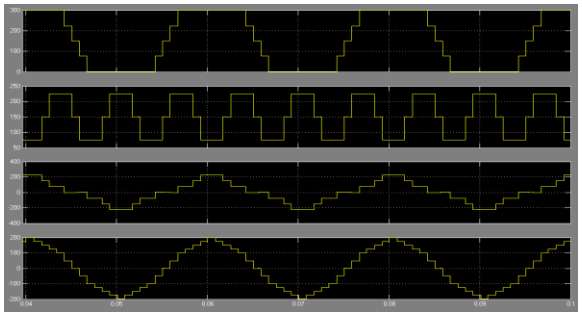

Fig. 3. Simulated waveforms of Vag, Vog, Vao, and VaN for the proposed inverter f=50 Hz.

$$V_q = \frac{4V_{dc}}{3(N-1)}(2Sa - Sb - Sc) \quad (6)$$

$$V_d = \frac{4V_{dc}}{\sqrt{3}(N-1)}(Sc - Sb) \quad (7)$$

$$V = V_q - jV_d. \quad (8)$$

For all switching states presented in Table II, Fig. 4 show the space vector diagram for the proposed topology.

Switching algorithm

The staircase modulation can be simply implemented for the proposed inverter. Staircase modulation with selective harmonic is the most common modulation technique used to control the fundamental output voltage as well as to eliminate the undesirable harmonic components from the output waveforms. A iterative method such as the Newton–Raphson method is normally used to find the solutions to(N–1) nonlinear transcendental equations. The difficult calculations and the need of high-performance controller for the real application are the main disadvantages of such method. Therefore, an alternative method is proposed to generate the inverter's switching gate signals. It is easier to control the proposed inverter and achieve the required output voltage waveforms in terms of Sa, Sb, and Sc. The basis of the proposed method can be explained as following: For a given value of modulation index Ma and within a full cycle of the operation of the proposed inverter, the switching states Sa, Sb, and Scare determined instantaneously. The on-time calculations of Sa, Sb, and Sc directly depend on the instantaneous values of the inverter line-to-ground voltages. It is well known that the reference values of Vag, Vbg, and Vcg are normally given by

$$\begin{bmatrix} V_{ag\_ref} \\ V_{bg\_ref} \\ V_{cg\_ref} \end{bmatrix} = \frac{M_a * 4V_{dc}}{2} * \begin{bmatrix} \cos(wt) \\ \cos\left(wt - \frac{2\pi}{3}\right) \\ \cos\left(wt + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{4V_{dc}}{2} * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (9)$$

Where wt is the electrical angle. Or

$$\begin{bmatrix} V_{ag\_ref} \\ V_{bg\_ref} \\ V_{cg\_ref} \end{bmatrix} = \frac{M_a * 4V_{dc}}{2} * \begin{bmatrix} \cos(wt) \\ \cos\left(wt - \frac{2\pi}{3}\right) \\ \cos\left(wt + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{4V_{dc}}{2} * \left[1 - \frac{M_a}{6}\cos(3wt)\right] * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}. \quad (10)$$

From (10), it can be noticed that the third harmonic component is added to the three-line-to-ground voltages. The third harmonic injection may increase the inverter fundamental voltage without causing over modulation. As a result, Ma can reach to 1.15 and Sa, Sb, and Sc can be simply determined by integrating the reference line-to-ground voltages as

$$\begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} = \text{integer}\left(\frac{N-1}{4V_{dc}} * \begin{bmatrix} V_{ag\_ref} \\ V_{bg\_ref} \\ V_{cg\_ref} \end{bmatrix}\right). \quad (11)$$

Comparison of the proposed modulation method with the staircase modulation with the selective harmonic method shows that the proposed

modulation features less time and needs imple calculations. The inverter's operating switching states Sa, Sb, and Sc and corresponding switching gate signals based on the proposed modulation method are shown in Fig. 5. It is clear that the switching gate signals are generated within 24 different modes starting from (044) to (034). Since the proposed inverter has been designed to achieve five voltage levels, the modulation index must be within range0.9≤Ma ≤1.15. For modulation index Ma <0.9, only two dc voltage supplies 4Vdcand 2Vdcare utilized and the behavior of the proposed inverter becomes similar to the three-level multilevel inverter. Using (9)–(11) and substituting N=3, the inverter's operating switching states Sa, Sb, and Sc at Ma<0.9 can be defined. The operation principle of the proposed inverter at Ma<0.9 is illustrated in Table III. Fig. 6(a) and (b) shows the inverter line-to-line voltage waveforms at five different modulation indices including the over modulation operation Ma=0.8, 0.9, 1.05, 1.15, and 1.3.

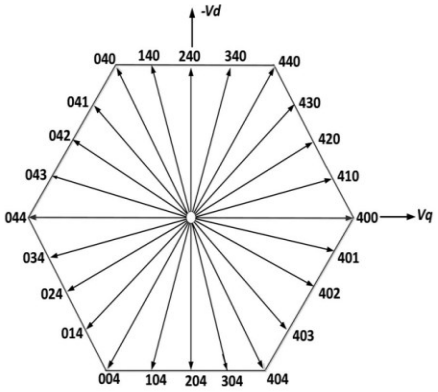

Fig. 4. Switching states vectors of the proposed inverter ind–q reference frame.

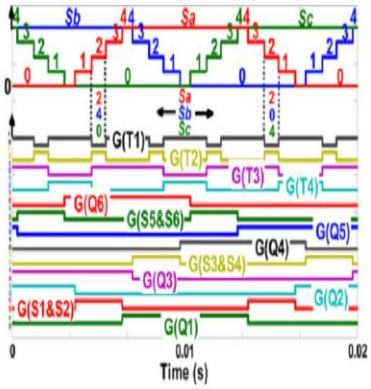

Fig. 5. Inverter's operating switching states Sa, Sb and Sc with corresponding witching gate signals based on the proposed modulation method.

TABLE III

SWITCHING STATES a1AND INVERTERLINE - TO-GROUND VOLTAGE Vag at Ma <0.9 (LEG a)

Sa1	Q1	S1	S2	Q2	T1	T2	T3	T4	*Vag*
2	on	off	off	off	off	on	on	off	*+4Vdc*
1	off	on	on	off	off	on	on	off	*+2Vdc*
0	off	off	off	on	off	on	on	off	*0*

Extended structure

It is noticeable that there is possibility to reach an output voltage with higher number of steps in the proposed multilevel inverter by extending the CHB circuit. Such extending can be done by adding more half-bridge cells connected in series as shown in Fig. 7(a) and (b). In order to achieve the desired number of voltage levels, three methods can be followed to determine the magnitudes of utilized dc voltage supplies. 1) All cells have an equal dc supply in magnitude.

$$V_{\mathrm{dc1}} = V_{\mathrm{dc2}} = \cdots = V_{\mathrm{dcn}} = V_{\mathrm{dc}}. \quad (12)$$

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Then, the magnitude of fixed dc supply can be chosen as

$$V_{\text{fix}} = (N-1)V_{\text{dc}} = (1+n)V_{\text{dc}} \quad (13)$$

Where n is the number of utilized cells. The maximum number Of voltage steps is related to the number of utilized cells by

$$N = n + 2. \quad (14)$$

The number of operation modes that makes the switching states sequence achieves the required output voltage waveform

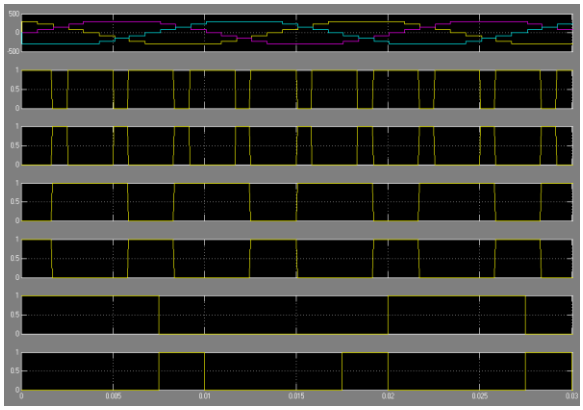

Fig. 6. Simulated waveforms of Vab at different modulation indices for the proposed inverter: (a)Ma =0.9, 1.05, and 1.15 and (b)Ma =0.8 and 1.3.]can be expressed as

$$M = 6(N-1). \quad (15)$$

2) The magnitude of dc voltage supply used in each and every cell in a particular inverter is obtained as follows:

$$V_{\text{dc1}} = V_{\text{dc}} \quad (16)$$

$$V_{\text{dc2}} = 2V_{\text{dc}} \quad (17)$$

$$V_{\text{dcn}} = nV_{\text{dc}} \quad (18)$$

$$V_{\text{fix}} = (N-1)V_{\text{dc}} = \left[1 + \frac{n(n+1)}{2}\right] V_{\text{dc}} \quad (19)$$

$$N = 2 + \frac{n(n+1)}{2} \quad (20)$$

$$M = 6(N-1). \quad (21)$$

3) By making a binary (power of 2) relationship between the dc supplies of the CHB structure as follows

(22)

$$V_{\text{dc2}} = 2^{(1)}(V_{\text{dc}}) \quad (23)$$

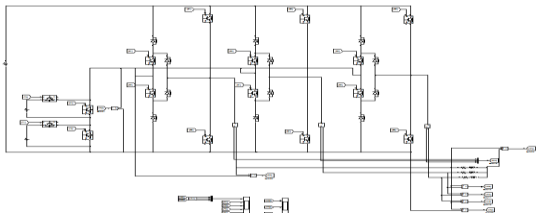

Fig. 7. Circuit diagram of the proposed three-phase N-levelmultilevelinverter

$$V_{\text{dcn}} = 2^{(n-1)}(V_{\text{dc}}) \quad (24)$$

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$$V_{\text{fix}} = (N-1)V_{\text{dc}} = \left[1 + \sum_{j=1}^{n} 2^{j-1}\right] V_{\text{dc}} = (2^n)V_{\text{dc}}$$

$$N = 1 + 2^n$$

(25
(26)

$$M = 6(N-1). \quad (27)$$

TABLE I V

COMPARISON OF THE MAXIMUM NUMBER OF VOLTAGE LEVEL WITH THE REQUIRED VALUE OF DC VOLTAGE SUPPLIES AMONG THE PROPOSED METHODS

Number of cells	1st method			2nd method			3rd method		
n	*N*	*M*	*Vfix*	*N*	*M*	*Vfix*	*N*	*M*	*Vfix*
2	4	18	*3Vdc*	5	24	*4Vdc*	5	24	*4Vdc*
3	5	24	*4Vdc*	8	42	*7Vdc*	9	48	*8Vdc*
4	6	30	*5Vdc*	12	66	*11Vdc*	17	96	*16Vdc*
5	7	36	*6Vdc*	17	96	*16Vdc*	33	192	*32Vdc*
6	8	42	*7Vdc*	23	132	*22Vdc*	65	384	*64Vdc*

.

Based on the comparison carried among the proposed methods, the following are some observations

1) Comparing to the second and third methods, the first method has a high modularity degree since the symmetric structure of CHB makes use of equal dc voltage supplies. This method helps the proposed inverter to reach all maximum number of voltage levels (4, 5, 6, 7, 8,...,N).

2) Since the second and third methods use the asymmetrical structure of CHB, the proposed inverter can reach the required output voltage and the maximum number of voltage levels such as 5, 8, 9, 12, 17,...with less number of dc voltage supplies and power electronic components.

Comparison study

In order to investigate the capability of the suggested configuration, the proposed inverter is compared with different types of multilevel inverters such as NPC, FC, and CHB. It is evident that the suggested three-phase N-level multilevel inverter can considerably minimize the required number of power components. For the same number of output voltage levels(N≥4),Table V explains the required number of dc voltage supplies ,switches, clamping diodes, control signals, and balancing capacitors of the proposed N-level inverter compared with three existing inverters NPC, FC, and CHB. As shown in Fig. 8,it can be noticed that nearly more than two-thirds of number of switches can be counted out as N increases. For instance, at the same number of voltage levels N=17, and compared with the existing multilevel inverters which require 96 switches, the required number of switches for the proposed inverter is less since it requires 42 switches based on the first method, 22switches based on the second method, and 20 switches based on the third method.

On the other hand, it is well known that the voltage and current ratings of the power components have an effect on the cost and realization of the multilevel inverter. Assuming that all power components have an equal current rating which is the rated current of the load (IL), the voltage ratings of these components depend on the magnitude of dc voltage supplies, voltage stress, and structure of the inverter. Considering that all inverters have the same input dc link which equals(N–1)Vdc, Table VI illustrates the rating requirements for the proposed inverter comparing with the rating requirements for the existing inverters. It is observed that the inverter employs switching devices with high voltage rating. That results in high cost per-switch. Since the topology is introduced with reduced number of switches, gate driver circuit, diodes and no clamping capacitors are involved, the semiconductor devices expenses are considerably recovered.

Power conversion efficiency and total harmonic distortion (THD%):

In order to determine the efficiency of the proposed inverter, it is necessary to determine the value of conduction and switching power losses generated by the semiconductor components. Basically, the main losses in semiconductor components such as IGBTs and diodes are categorized into two groups: conduction loss (Pcon) and switching loss (Psw)as follows

$$P_{\text{sw\_IGBT}} = \frac{1}{T}\int_0^T E_{\text{on}}(t)dt + \frac{1}{T}\int_0^T E_{\text{off}}(t)d(t) \quad (28)$$

$$P_{\text{sw\_diode}} = \frac{1}{T}\int_0^T E_{\text{rr}}(t)dt \quad (29)$$

Where Eon(t)is a turn-on loss and Eoff(t) is a turn-off loss. Switching losses Eon(t) and Eoff(t)are experienced during the ON and OFF states, respectively. While Err(t)is the reverse recovery loss of the diode, the majority of switching loss, which is experienced when the diode is turned OFF (OFF state)

$$P_{\text{con\_IGBT}} = \frac{1}{T}\int_0^T V_{\text{on\_IGBT}}\, i(t)dt \quad (30)$$

$$P_{\text{con\_Diode}} = \frac{1}{T}\int_0^T V_{\text{on\_diode}}\, i(t)dt. \quad (31)$$

Conduction power losses of IGBT and diode are approximated based on their forward voltage drops Von IGBT, Von diode, and the instantaneous current i(t) flowing through IGBT or diode. The total losses P t are expressed as follows:

$$P_t = P_{\text{con}} + P_{\text{sw}}. \quad (32)$$

Once the total semiconductors losses Pt in the introduced inverter are defined, the relative inverter efficiency is determined based on the following expression:

$$\eta\% = \frac{P_{\text{out}}}{P_t + P_{\text{out}}} \times 100. \quad (33)$$

Table VII provides the possible current directions with corresponding conducting devices in phase a. MATLAB/Simulink model of the proposed inverter shown in Fig. 1 has been developed to study the conduction and switching power losses. The proposed inverter is designed to deliver output power of Pout=1.9 kW. Three-phase series resistive–inductive (23Ω–3 mH/Phase) in star connection is used as load. The multilevel dc link is determined as Vdc=75 V, 2Vdc=150 V, and Vfix =4Vdc =300 V and the proposed staircase modulation technique at Ma=1 is implemented to generate the appropriate switching gate signals. Three different types of semiconductor components are selected to build the prototype of the proposed inverter power circuit as following: IGBT (HGTG20N60B3D) 600 V/40 A for the two-level bridge and CHB switches, IGBT (IRG4BC40W) 600 V/20 A for bidirectional switches, and Diode (RHRP1540) 400 V/15 A for embedded diodes in bidirectional switches and freewheeling diodes. The data sheets of the utilized semiconductor components are easily accessed to acquire their characteristics curves. To simplify the losses calculation, a curve-fitting tool of MATLAB is used to approximate these curves by exponential equations [35]. The mathematical models obtained for HGTG20N60B3D 600 V/40 A are given by

$$V_{\text{on\_IGBT1}} = 1.418e^{0.016i(t)} \quad (34)$$

$$E_{\text{on\_IGBT1}} = \left(201.6e^{0.04418i(t)} - 291.6e^{-0.1265i(t)}\right) \times 10^{-6} \quad (35)$$

$$E_{\text{off\_IGBT1}} = \left(323.9e^{0.05125i(t)}\right) \times 10^{-6}. \quad (36)$$

While the mathematical models obtained for IRG4BC40W 600 V/20 A are given by

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$$E_{\text{sw\_IGBT2}} = (0.3405e^{0.04472i(t)}) \times 10^{-3}.$$

$$V_{\text{on\_IGBT2}} = 1.555e^{0.0085371i(t)} \quad (37)$$

(38)

And finally, the mathematical models obtained for RHRP1540 400 V/15 A are given by

$$V_{\text{on\_diode}} = 1.325e^{0.006424i(t)} - 0.8571e^{-0.07183i(}$$

(39)

$$E_{\text{rr\_diode}} = (15.7e^{-0.002733i(t)} + 2.74e^{-0.1413i(t)} - 3.162e^{-0.05923i(t)} - 8e^{-0.09452}) \times 10^{-6}. \quad (40)$$

TABLE V

Comparison of the proposed n-level inverter with the existing inverters

Converter type	NPC	FC	CHB	Proposed		
				1st method	2nd method	3rd method
Switches	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+10$	$\sqrt{8N-15}+11$	$2Log_2(N-1)+12$
Gate drivers	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+7$	$\sqrt{8N-15}+8$	$2Log_2(N-1)+9$
Diodes	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+10$	$\sqrt{8N-15}+11$	$2Log_2(N-1)+12$
Clamping diodes	$6(N-2)$	0	0	0	0	0
DC supplies	$N-1$	$N-1$	$3(N-1)/2$	$N-1$	$1+[(\sqrt{8N-15}-1)/2]$	$1+Log_2(N-1)$
Clamping capacitors	0	$3(N-2)$	0	0	0	0
Control signals	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+7$	$\sqrt{8N-15}+8$	$2Log_2(N-1)+9$

Therefore, the conduction and switching power losses for the inverter switches and diodes can be estimated by substituting (34)–(40) into (28)–(33). The efficiency of the proposed inverter is estimated while the input voltage is raised in small steps. Fig. 9(a) depicts the estimated value of efficiency over a wide range of the output power. It is clear that the inverter's efficiency varies directly proportional to the output power and reaches its maximum value of 96.53% at 1.9 kW. It is a result of more power being effectively transferred with respect to the power losses. Furthermore, the power losses distribution among the inverter's legs and the CHB cells are shown in Fig. 9(b). The power losses distribution is obtained during the operation of the proposed inverter to deliver Pout=1.287 kW at voltage step Vdc=62.5 V, 2Vdc=125 V, and Vfix=4Vdc=250 V. The power losses generated by legs a, b, and care almost equal and slightly higher than those generated by CHB cells. According to Fig. 9(b), 53.3% of the total value of power loss is experienced in the conventional two-level bridge since 3×9.92 W in term of conduction power losses is generated by Q1–Q6. It is definitely due to fact that the conduction power loss is directly proportional to the switch conduction time and the value of conducting current (for instance, Q1 and Q2 conduct the load current in 18 modes). Negligible conduction power losses are generated by the free whiling diodes (D1–D6). Further measurements show that 9.68+2.2 W is the estimated value of the conduction power losses generated by CHB's switches and diodes. It is almost 21.3% of total power loss. The higher conduction power loss is experienced in T3 followed by T1, T4, and T2. The three bidirectional switches contribute to 19.6% of the total power loss as 3×3.66 W is the estimated value of conduction power loss generated by S1–S6 and Da1–Dc2. Finally, it can be observed that a negligible switching loss is generated since the fundamental frequency is implemented. Furthermore and in order to assess the performance of the proposed inverter comparing with other type of the multilevel inverter, a five-level NPC multilevel inverter built by IRG4BC40W 600 V/20 A and RHRP1540 400 V/15 A semiconductor component types has been modeled and operated under the same conditions to the proposed inverter. The estimated value of efficiency and power losses distribution of the NPC multilevel inverter are shown in ig. 9(c) and (d). Comparison of the proposed inverter' efficiency with the five-level NPC multilevel inverter's efficiency shows that the proposed inverter has a higher efficiency since the

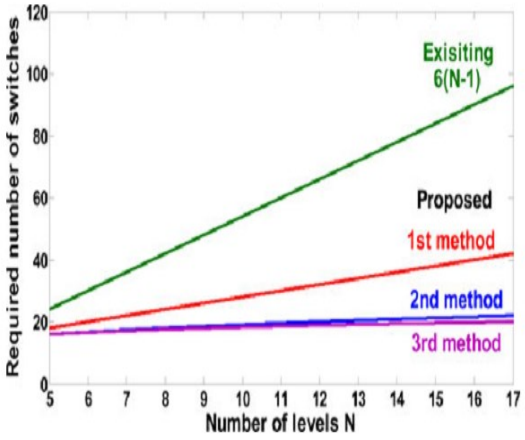

Fig. 8. Comparison of required number of switches among existing inverters and the proposed topology

TABLE VI

Proposed and the existing topologies rating requirements per level n

Proposed inverter	Main bridge Q1 ~ Q6 D1a ~D2c	Bidirectional switches S1 to S6 D1 to D6	Cascaded half-bridge switches T11 to Tn2			Converter type	NPC	FC	CHB
			1st method	2nd method	3rd method	switches voltage rating	*Vdc*	*Vdc*	*Vdc*
Component voltage rating	(N-1)*Vdc*	(N-2) *Vdc*	*Vdc*	*nVdc*	$2^{(n-1)}$ *Vdc*	Clamping diode voltage rating	*Vdc*	0	0
						Clamping capacitor voltage rating	0	*Vdc*	0
Active Component current	*IL*	*IL*	*IL*	*IL*	*IL*	Active component current	*IL*	*IL*	*IL*

TABLE VI I

Conducting devices of the proposed inverter phase a

Current	Conducting Devices Phase *a*. Fig. 1(a)	*Vag*	Conducting Devices Phase *a*. Fig. 1(b)	*Vag*
Ia > 0	Q1	+4*Vdc*	Q1	+4*Vdc*
	T1, T3, S2, Da2	+3*Vdc*	T1, T3, S2, Da2	+3*Vdc*
	Dz2, T3, S2, Da2	+2*Vdc*	Dz2, T3, S2, Da2	+2*Vdc*
	T1, Dz4, S2, Da2	+*Vdc*	T1, Dz4, S2, Da2	+*Vdc*
	D2, Da2	0	D2	0
Ia < 0	D1, Da1	+4*Vdc*	D1	+4*Vdc*
	Dz1, Dz3, S1, Da1	+3*Vdc*	Dz1, Dz3, S1, Da1	+3*Vdc*
	T2, Dz3, S1, Da1	+2*Vdc*	T2, Dz3, S1, Da1	+2*Vdc*
	Dz1, T4, S1, Da1	+*Vdc*	Dz1, T4, S1, Da1	+*Vdc*
	Q2	0	Q2	0

Fig. 9. Power loss and efficiency comparison. For the proposed inverter: (a) output power versus efficiency, (b) Pcon and Psw distribution among legs a, b, c, and CHB cells for Ma=1andPout=1.287 kW. For the NPC inverter: (c) output power versus efficiency and (d)Pcon and Psw distribution among leg sa, b, and c for Ma =1andPout=1.285 kW maximum estimated efficiency of the NPC multilevel inverter is 93.85%. The lower Pt generated by the proposed inverter comparing with Pt generated by the five-level NPC multilevel inverter is a result of the low conduction power losses and reduced number of power components. A lower voltage stress leads to a lower switching power loss. However, the more the switching devices, the higher the conduction power losses. At the same operating pointPout≈1.287 kW and compared with the estimated value of Pt proposed=3×14.4+12.78≈55.9 W generated by the proposed inverter, the estimated value of P generated by the NPC multilevel inverter is two times higher.

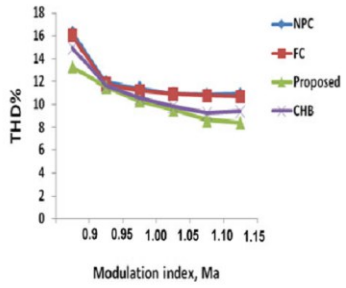

Fig. 10. NPC, FC, CHB, and proposed inverter: line-to-line voltage THD% versus Ma.

It is nearly Pt NPC=3×37.5≈112.5 W. Moreover, the proposed inverter has been tested under different modulation indices (Ma =0.9, 1, and 1.15). THD% of the output voltage can be calculated **by**

$$\mathrm{THD\%} = \frac{\sqrt{\sum_{k=2}^{\infty} V_k^2}}{V_1} \times 100\% \qquad (41)$$

Where V1 and Vk are the fundamental component and harmonic order, respectively. NPC, FC, and CHB multilevel inverters have been tested under the same operating conditions. The goal of this test is to

compare the proposed inverter with the existing inverters in term of THD%. Fig. 10 depicts THD% of the line-to line voltage for all inverters within specific range of modulation indices [0.9–1.15]. It can be seen that the THD% of all inverter is slightly different. The measured values of THD% for the proposed inverter are within a range of 8.4–13.25%. As a result, the proposed inverter essentially adds the attractive aspects of the traditional two-level inverter such as less power components, simple working principle, and minimum conduction power loss to the main advantages of the multilevel inverter such as low THD% and high output voltage quality.

CONCLUSION

A new topology of the three-phase five-level multilevel inverter was introduced. The suggested configuration was obtained from reduced number of power electronic components. Therefore, the proposed topology results in reduction of installation area and cost. The fundamental frequency staircase modulation technique was comfortably employed and showed high flexibility and simplicity in control. Moreover, the proposed configuration was extended to N-level with different methods. Furthermore, the method employed to determine the magnitudes of the dc voltage supplies was well executed. In order to verify the performance of the proposed multilevel inverter, the proposed configuration was simulated and its prototype was manufactured. The obtained simulation and hardware results met the desired output. Hence, subsequent work in the future may include an extension to higher level with other suggested methods. For purpose of minimizing THD%, a selective harmonic elimination pulse width modulation technique can be also implemented.

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CHENNAIAH BANOTH

Completed **B.Tech**. in Electrical & Electronics Engineering in 2008 from VAAGDEVI COLLEGE OF ENGINEERING, Bollikunta,Warangal Dist, Affiliated to JNTUH, Hyderabad, Telangana, India. and **M.Tech** in Power Electronics(PE) in 2011 from VAAGDEVI COLLEGE OF ENGINEERING, Bollikunta, Warangal Dist, Affiliated to JNTUH, Hyderabad, Telangana, India Area of interest includes Power Electronics, Building Electrical services and Building Automation.

E-mail id: banoth.chennaiah@gmail.com

MAHENDER KODELA

Completed B.Tech in Electrical & Electronics Engineering in 2009 from Vaagdevi college of Engineering, warangal Affiliated to JNTUH, Hyderabad and M.Tech in Power Electronics in 2013 from SR Engineering College, Warangal. Working as Assistant Professor at Vaagdevi College Of Engineering, warangal, Telangana, India. Area of interest includes Power Electronics,Control SyStems.
E-mail id: mahi.kodela@gmail.com

KUMARASWAMY MADAVENA

Completed B.Tech in Electrical & Electronics Engineering in 2008 from Vaagdevi college of Engineering, warangal Affiliated to JNTUH, Hyderabad and M.Tech in Control Systems in 2011 from Ramappa Engineering College, Warangal. Telangana, India. Working as Assoc. Professor at Ganapathi Engineering College, warangal, Telangana, India. Area of interest includes Power Electronics, Control Systems.
E-mail id : kumar21sriram@gmail.com

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