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Diode Clamped Multilevel Inverter Fed Induction Motor For Advanced Modulating Techniques

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***Abstract*—** In this context, the multilevel inverters with larger number of levels suitable for circuit integration are actively investigated. Diode-clamped multilevel inverters are regarded as the promising solution. As the number of voltage levels increases the harmonic content decreases significantly.The general function of the multilevel inverter is to synthesize a desired AC voltage from several levels of DC voltages. Multilevel inverters are mainly used in medium voltage and high power applications to reduce the required voltage rating of the power semiconductor switching devices. These multilevel inverters are used to increase inverter operating voltage, to minimize THD with low switching frequency, to reduce EMI due to lower voltage steps. The advantages of this multilevel approach include good power quality, good electromagnetic compatibility, low switching losses and high capability. This project proposes to study various multilevel inverter topologies, to simulate various modulating techniques for diode clamped multi level inverter fed induction motor. These modulating techniques include sinusoidal pulse width modulation, modified reference modulating techniques. i.e., trapezoidal reference, staircase reference, stepped reference, third harmonic injected reference and offset line voltage injected reference with triangular carrier waves. The main objective of this study is to reduce total harmonic distortion, comparison of THD and fundamental component for different modulation techniques. The Simulated Induction motor model is connected at the end to observe the Stator current harmonics and speed-torque characteristics.

Keywords: induction motor, diode clamped multi level inverters, multi level carrier signals, modulation, total harmonic distortion.

I. INTRODUCTION

Traditional two level and three level high frequency pulse width modulation (PWM) inverters for motor drives have several problems associated with high frequency switching, which produce common-mode voltages and high voltage change (dv/dt) rates to the motor windings. The concept of utilizing multiple small voltage levels to perform power conversion was introduced. These converters recently have found many applications in the medium and high power applications. Recent advances in power electronics made the multilevel concept practical [8, 10]. In fact, the multilevel is so advantageous that several major drives manufacturers have obtained recent patens on multilevel power converters and associates switching techniques. Furthermore, several IEEE conferences now hold entire session on multilevel conversion. It is evident that the multilevel concept will be a prominent choice for power electronic systems in future years, especially for medium-voltage operations

DC motors have been used during the last century in industries for variable speed control applications, because its flux and torque can be controlled easily changing the field and armature currents respectively. Furthermore, four quadrant operation of induction motor was also achieved. Induction motor is popularly used in industries due to ruggedness and robustness. The induction motors were mainly used for essentially constant speed applications because of the unavailability of the variablefrequency voltage supply. The advancement of power electronics has

made it possible to vary the frequency of the voltage. Thus, it has extended the use of induction motor in variable speed drive applications. The concept of multilevel inverter control has opened a new possibility that induction motors can be controlled to achieve dynamic performance equally as that of DC motors.

Depending on voltage levels of the output voltage waveforms, the inverters can be classified as Two-level inverters and Multi-level inverters. The inverters with voltage level 3 or more are referred as Multi-level inverters. Multi-level inverters have been attracting recently, particularly because of the increased power ratings, improved harmonic performance and reduced EMI emission that can be achieved with the multiple DC levels that are available for synthesis of the output voltage waveforms.

Pulse width modulation (PWM) control strategies development concerns the development of techniques to reduce the total harmonic distortion (THD) of the current [1]. PWM techniques can be broadly classified into two categories depending on the method of switching signal generation, there are Sine triangle PWM (SPWM) and Space Vector PWM (SVPWM). Even though the principle of five-level SVPWM is similar that of three-level SVPWM, the five-level SVPWM algorithm is complicated compared to two-level inverters and three-level inverters due to more number of switching states. Because of above reason the simulation of five-level inverter can be done by using Modified SVPWM.

2. MULTILEVEL CONCEPT A three-phase inverter system [4], as shown in Figure-1, with a dc voltage Vdc. Series-connected capacitors constitute the energy tank for the inverter, providing some nodes to which the multilevel inverter can be connected. Each capacitor as the same voltage Em, which is given by

multilevel converter system for a high power application [1-3]. The concept of multilevel converters has been introduced since 1975 [4]. The term multilevel began with the three-level converter [5]. Subsequently, several multilevel converter topologies have been developed [6-13]. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows. ● Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced. ● Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [14]. ● Input current: Multilevel converters can draw input current with low distortion. ● Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

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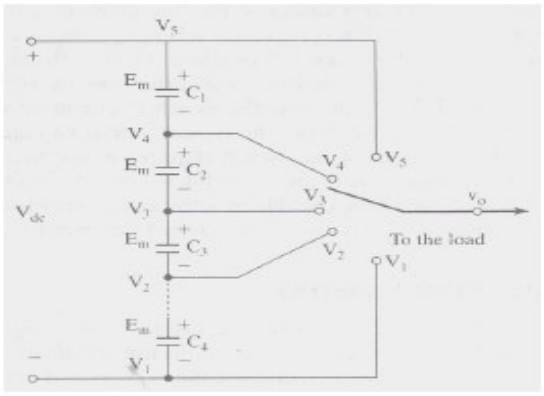

Fig.1 Typical Circuit Topologies of Three-phase multilevel power processing system Multilevel Inverters.

The multilevel inverters can be classified into three types [5]. Diode-clamped multilevel inverter. Flying-capacitors multilevel inverter. Cascade multilevel inverter.Diode clamped multi level inverter (DCMLI) The most commonly used multilevel topology is the diode clamped inverter [4], in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Figures 2 and 3 show the circuit for a diode clamped inverter for a three-level and a five-level inverter. The key difference between the two-level inverter and the three-level inverter are the diodes D1a and D2a. These two devices clamp the switch voltage to half the level of the DC bus voltage. In general the voltage across each capacitor for an m-level diode clamped inverter at steady state is Vdc/m-1. Although each active switching device is only required to block Vdc/m-1, the clamping devices have different ratings. The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the DC bus, so the terminology neutral point clamped (NPC) inverter was introduced. However, with an even number of voltage levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied. Due to capacitor voltage balancing issues, the diodeclamped inverter implementation has been limited to the three levels. Because of industrial developments over the past several years, the three-level inverter is now used extensively in industry applications.

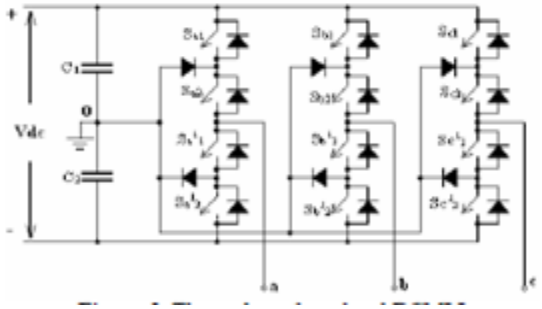

Figure-2 Three Phase three-level DCMLI

The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m level diode-clamp inverter needs (m-1) capacitors on the DC bus. A three-phase three-level diode-clamped inverter is shown in Figure-2. In this circuit, the DC bus voltage is split in to three levels by two series connected bulk capacitors C_1 and C_2. The middle point of the two capacitors 'n' can be defined as the neutral point. The diodes D_{a1} and D_{a2} clamp the switch voltage to half the level of the DC bus voltage.

A three-phase five-level diode-clamped inverter is shown in Figure-3. In this circuit, the dc bus voltage is split in to five levels by four series connected bulk capacitors C_1, C_2, C_3 and C_4. For a dc bus voltage Vdc, the voltage across each capacitor is Vdc/4, and each device voltage stress will be limited to one capacitor voltage level, Vdc/4, through clamping diodes.

For the general case of an m-level topology, one phase leg consists of 2(m-1) active switches and (m-1) (m-2) clamping diodes, where m is the number of voltage levels shown in Figure-4. The total dc bus voltage Vdc is distributed across the dc capacitors C_1, $C_{2 \ldots C (m-1)}$. Hence, an output voltage of -Vdc / (m-1), Vdc / (m-1) is possible at the output.

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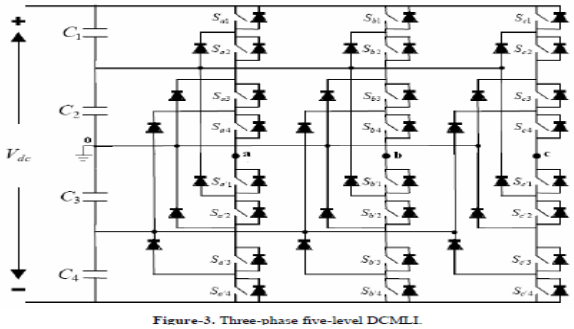
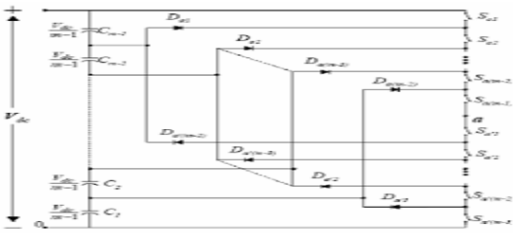


Figure-3. Three-phase five-level DCMLI.

Figure-3. Three-phase five-level DCML



3. MODULATION TECHNIQUES

Pulse width modulation (PWM) control strategies development concerns the development of techniques to reduce the total harmonic distortion (THD) of the current. It is generally recognized that increasing the switching frequency of the PWM pattern reduces the lower-frequency harmonics by moving the switching frequency carrier harmonic and associated sideband harmonics further away from the fundamental frequency component. While this increased switching frequency reduces harmonics, resulting in a lower THD by which high quality output voltage waveforms of desired fundamental r.m.s value and frequency which are as close as possible to sinusoidal wave shape can be obtained. Any deviation from the sinusoidal wave shape will result in harmonic currents in the load which result in electromagnetic interference (EMI), harmonic losses and torque pulsation in the case of motor drives. The quality of the output waveform will improve with increase in switching frequency. Higher switching frequency can be employed for low and medium power inverters, whereas, for high power and medium voltage applications the switching frequency is of the order of 1 kHz.

One of the most important problems in controlling a VSI with variable amplitude and frequency of the output voltage is to obtain an output waveform as much as possible of sinusoidal shape employing simple control techniques. Indeed, current harmonics caused by non-sinusoidal voltage feeding imply power losses, electromagnetic interference (EMI), and pulsating torques in ac motor drives. Harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy.

Under the aspect of harmonic content reduction, multilevel inverters are of the highest importance. They are particularly suitable in high-power applications when the semiconductor devices are not able to operate at high switching frequencies. It is also worth noting that, when solid-state switches, which further lower the highest possible switching frequencies. The multilevel structures allow raising the power handled in the conversion processes, in a very natural and powerful way. The inverter control of three-phase six-step inverter is simple and switching loss is low because there are only six switching per cycle of fundamental frequency. Because an inverter contains electronic switches, it is possible to control the output voltage as well as optimize the harmonics by performing multiple switching within the inverter with the constant dc input voltage Vdc.

Sinusoidal pulse width modulation (SPWM)

In sinusoidal PWM instead of maintaining the width of all pulses the same as in the case of multiple PWM, the width of each is varied in proportion to the amplitude of a sine wave evaluated at the same pulse. The distortion is reduced significantly compared to multiple PWM

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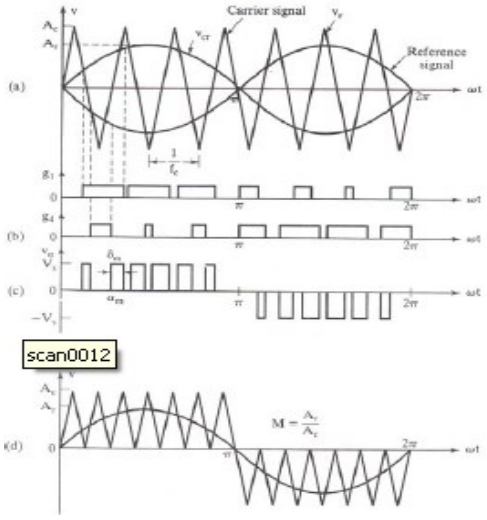

Figure-5. Sinusoidal pulse width modulation.

A high frequency triangular wave, called the carrier wave, is compared to a sinusoidal signal representing the desired output, called the reference wave. Usually, ordinary signal generators produce these signals. Whenever the carrier wave is less than the reference, a comparator produces a high output signal, which turns the upper transistor in one leg of the inverter on the lower switch off. In the other case the comparator sets the firing signal low, which turns the lower switch ON and upper switch OFF.

The number of pulses per half cycle depends on the carrier frequency. Within the constraint that two transistors of the same arm cannot conduct at same time, the instantaneous output voltage is shown in Figure-5 the same gating signals can be generated by using unidirectional triangular carrier wave as in Figure-5 this method is preferable and easier to implement. The output voltage can be varied by varying the modulation index 'm'. The area of each pulse corresponds approximately to the area under the sine wave between the adjacent mid points of off-periods on the gating signals.

The SPWM, which is most commonly used, suffers from certain drawbacks like low fundamental output voltage. The other techniques offer improved performances are

- Trapezoidal modulation.
- Staircase modulation
- Stepped modulation
- Third Harmonic injected modulation
- Space Vector Pulse width Modulation

Trapezoidal modulation

In this technique the gate signals are generated by comparing a triangular carrier wave with a modulating Trapezoidal wave as shown in Figure-6. The Trapezoidal wave can be obtained from a triangular wave by limiting its magnitude to $A_{r,}$ which is related to the peak value $A_{r\,max}$ by

$A_r = \sigma A_{r\,max}$

Where σ is called the triangular factor, because the waveform becomes a triangular wave σ =1. The modulation index is

M = = for 0 M1

The angle of the flat portion of the trapezoidal wave is given by

$2\Phi = (1-\sigma)\ \pi$

The fixed values of $A_{r\ max}$ and Ac, M that varies with the output voltage can be varied by changing the triangular factor 'σ'.

Staircase pulse width modulation

The modulation signal is a stair case wave as shown in Figure-7. The stair case is not a sampled approximation to the sine wave. The levels of the stairs are calculated to eliminate specific harmonics. The modulation frequency ratio m_f and the numbers of steps are chosen to obtain the quality of output voltage.

This is an optimized PWM and is not recommended for fewer than 15 pulses in one cycle. It has been shown that for high fundamental output voltage and low distortion factor. The optimum number of pulses in one cycle is 15 for two levels, 21 for three levels and 27 for four levels. This type of control provides a high quality output voltage with a fundamental value of up to 0.94 V_s.

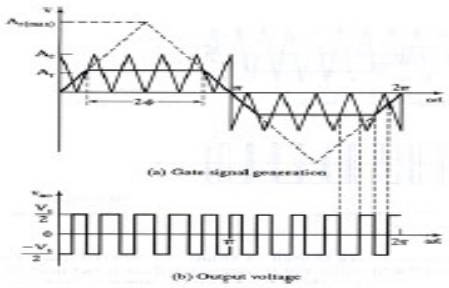

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Figure-6. Trapezoidal PWM.

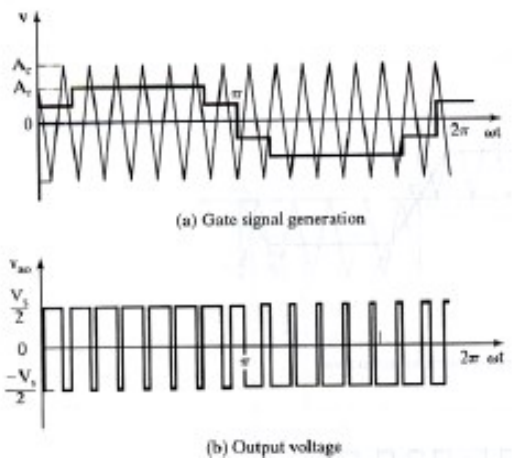


Figure-7. Staircase modulation.

Stepped modulation

The modulating signal is a stepped wave as shown in Figure-8.

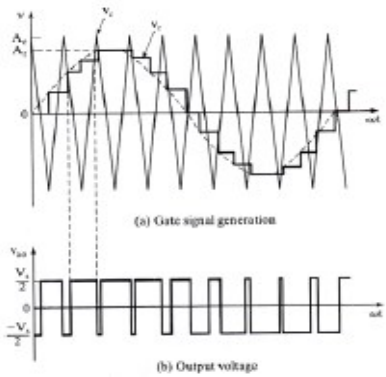


Figure-8. Stepped modulatio

The stepped wave is not a sampled approximation to the sine wave. It is divided into specified intervals, say 20°, with each interval controlled individually to control the magnitude of the fundamental component and to eliminate specific harmonics. This type of control gives low distortion, but higher fundamental amplitude compared with of normal PWM control.

Third harmonic injected PWM

It is implemented in the same manner, as sinusoidal PWM. The difference is that the reference ac waveform is not sinusoidal but consists of both fundamental component and a third-harmonic component. As a result, the peak -to-peak amplitude of the resulting function does not exceed the dc supply voltage V_s, but the fundamental component is higher than the available supply voltage V_s.

The presence of exactly the same third-harmonic component in each phase results in an effective cancellation of the harmonic component in the neutral terminal, and the line-to-neutral phase voltages (V_{an},V_{bn}, V_{cn}) are all sinusoidal with peak amplitude of $V_p = V_s/\sqrt{3}=0.57735$ Vs. The fundamental component is the same peak amplitude $V_{p1}=0.57735$ Vs and the peak line voltage is $V_L=\sqrt{3} V_p = \sqrt{3}*0.57735$ Vs = Vs. This is approximately 15.5% higher in amplitude than that achieved by the sinusoidal PWM. Therefore, the third-harmonic PWM provides better utilization of the dc supply voltage than the sinusoidal PWM does

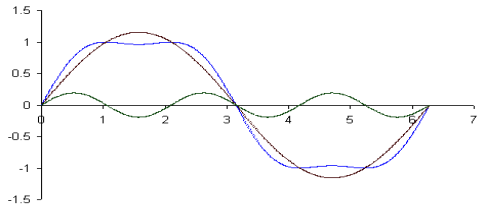


Figure-9. Third harmonic injected PWM.

Space vector pulse width modulation (SVPWM)

SVPWM is a digital modulating technique where the objective is to generate, PWM load line voltages that are in average equal to a given reference load line voltages. With PWMs, the inverter can be thought of as three separate push pull driver stages, which create each phase waveform independently. SVM treats the inverter as a single unit; specially, the inverter can be driven in to eight unique states as shown in Table. Modulation is accomplished by switching the state of the inverter. SVM can be implemented by properly selecting the switch states of the inverter and the calculation of the appropriate time period for each state in each sampling period.

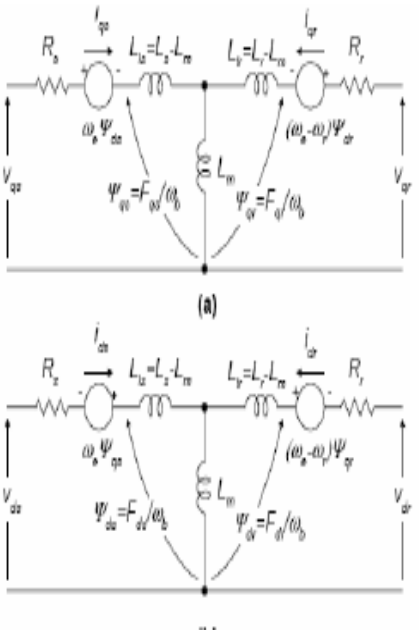
4. MODELLING OF INDUCTION MOTOR

AC induction motor is the most common motor used in industry and mains powered home appliances. Induction motors are also some times

called squirrel cage motors because the appearance of early rotors. This type of industrial AC electric motor, being rugged and requiring neither a separate DC power source nor slip-rings. AC induction motors offer users simple, rugged construction and easy maintenance. An induction motor consists of two basic assemblies-stator and rotor-and is analogous to an ac transformer with a rotating secondary. The motors name comes(s) from the alternating current (ac) induces into the rotor by rotating magnetic flux produced in the stator. Motor torque is developed from interaction of currents flowing in the rotor bars and the stator's rotating magnetic field. Protection of induction motors is necessary to avoid motor failures when something goes wrong. It is somewhat hard to protect an AC induction motor against overload with normal fuses, because at startup those motors take, for some time, much higher current than is allowed for continuous operation. The thermal overload relays are suitable for overload protection of AC motor operated on hours duty or uninterrupted duty. There are also more advanced protection relays which provide phase-failure protection, temperature compensation, ON/OFF indication and manual/automatic reset. In order to reduce the downtime of motors used in industrial plants, high performance circuit breakers can be utilized to switch off and on overheated motors without the need for manual intervention of service personnel. Testing, integration and validation of complex controlled systems have been traditionally made in a systematic way consisting of analyzing the behavior of individual components, mostly by simulation. In several cases, the integration is directly made with prototypes of the real equipments. At this stage, real cautions were to be taken because of the power levels: a simple controller malfunction could damage the prototype or the real systems and create project delays and cost increases. The analysis of their performance is often required in power system studies. The analysis is either concerned with steady-state performance or with transient performance during start-up and during system disturbances.

The per phase equivalent circuit of the induction motor can be used for only steady state analysis. The induction motor contains time varying mutual inductances in the transient state which makes the analysis using per phase equivalent circuit and impossible one. The analysis using d-q model can take care of the time varying quantities in the transient state. Usually, when an electrical machine is simulated in circuit simulators like PSpice, its steady state model is used, but for electrical drive studies, the transient behavior is also important. One advantage of Simulink over circuit simulators is the ease in modeling the transients of electrical machines and drives and to include drive controls in the simulation.

The induction machine d-q or dynamic equivalent circuit is shown in Figure-10.



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The modeling equations in flux linkage form are as follows:

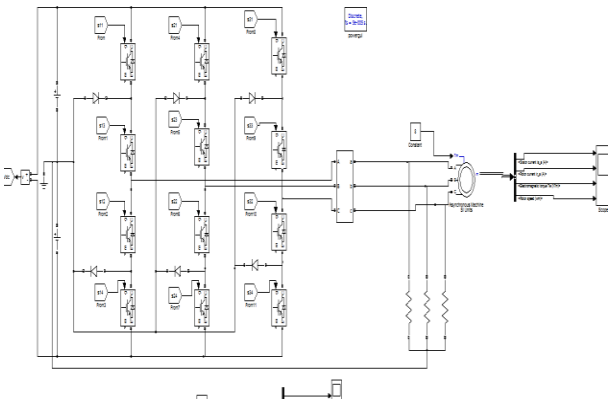
$$\frac{dF_{qs}}{dt} = \omega_b \left\{ v_{qs} - \frac{\omega_e}{\omega_b} F_{ds} + \frac{R_s}{x_{ls}} \left(F_{mq} + F_{qs} \right) \right\}$$

$$\frac{dF_{ds}}{dt} = \omega_b \left\{ v_{ds} + \frac{\omega_e}{\omega_b} F_{qs} + \frac{R_s}{x_{ls}} \left(F_{md} + F_{ds} \right) \right\}$$

$$\frac{dF_{qr}}{dt} = \omega_b \left\{ v_{qr} - \frac{\omega_e - \omega_r}{\omega_b} F_{dr} + \frac{R_r}{x_{lr}} \left(F_{mq} - F_{qr} \right) \right\}$$

$$\frac{dF_{dr}}{dt} = \omega_b \left\{ v_{dr} + \frac{\omega_e - \omega_r}{\omega_b} F_{qr} + \frac{R_r}{x_{lr}} \left(F_{md} - F_{dr} \right) \right\}$$

5. SIMULATION RESULTS FOR 3-LEVEL AND 5-LEVEL DCMLI



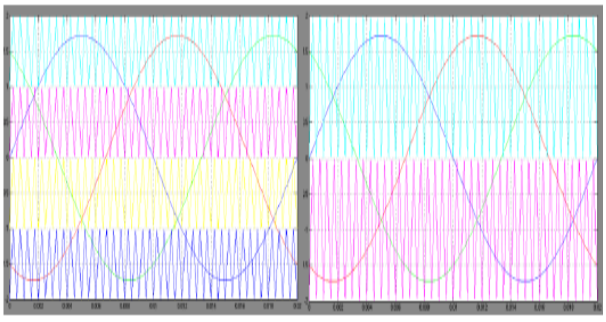


Figure-11. Simulated output of sinusoidal PWM.

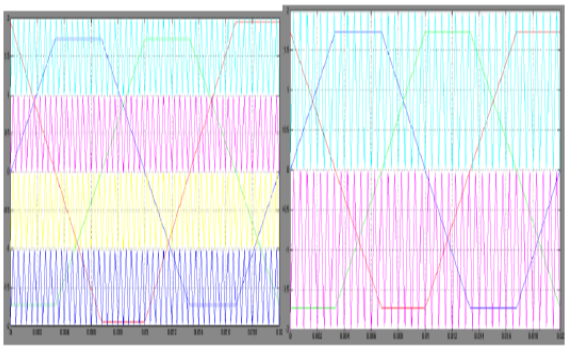


Figure-12. Simulated output of Trapozoidal PWM.

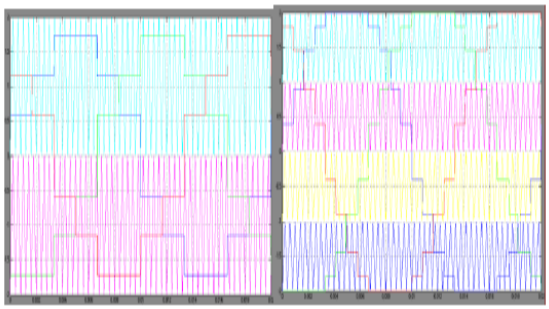


Figure-13. Simulated output of staircase PWM.

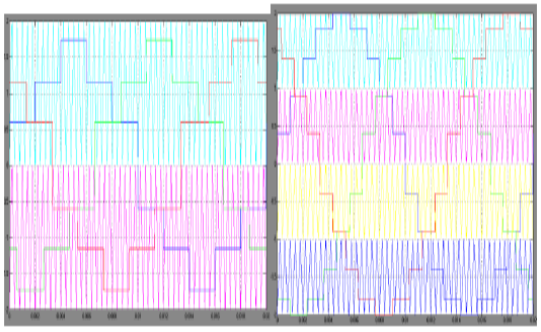


Figure-14. Simulated output of stepped PWM.

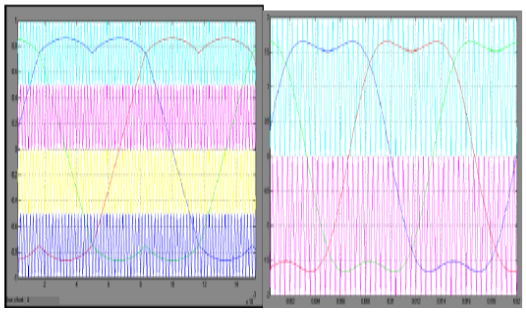


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Figure-15. Simulated output of third harmonic injected PWM.

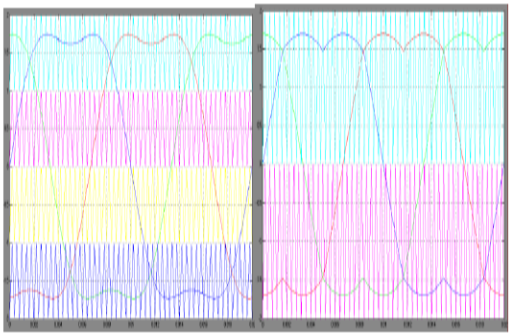

Figure-16. Simulated output of offset voltage injected PWM.

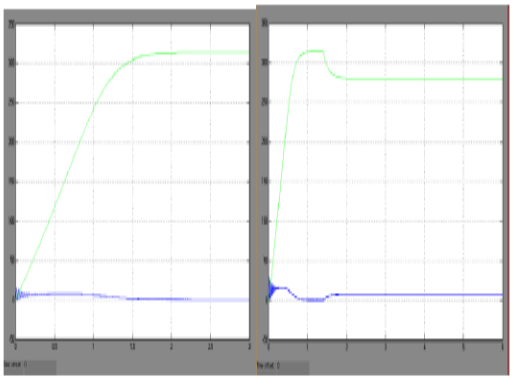

Figure-17. Speed and torque characteristics of IM NO load and load of 8 N-m.

Modulation Technique	3-level			5-level		
	Line voltage THD	Stator current THD	Fundamental voltage (volts)	Line voltage THD	Stator current THD	Fundamental voltage (volts)
SPWM	44.3%	4.03%	269.9	16.97%	2.55%	288.9
Trapizoidal	40.08%	2.55%	299.8	18.39%	1.72%	312.8
Stair case	44.53%	2.55%	302.8	17.13%	1.58%	336.3
Stepped	36.68%	2.08%	317.6	16.77%	1.5%	331.3
Third harmonic	35.62%	1.38%	332.6	17.03%	0.77%	345.7
Offset voltage	34.84%	1.23%	346.3	16.38%	0.74%	346.6

V. CONCLUSIONS

The simulation results of Diode Clamped five-level inverter fed induction motor with various modulating techniques are implemented through MATLAB/ SIMULINK. The output quantities like line-line voltage, Stator current waveform, the THD spectrum for line-line voltage, stator current and torque speed characteristics of induction motor are obtained. The best performance is achieved for the offset voltage injected PWM.

REFERENCES

[1] T. Ohnishi and H. Okitsu. 1983. A novel PWM technique for three-phase inverter/converter. International Power Electronics Conference. pp. 384395.

[2] T.P. Chen, Y.S. Lai and C.H. Liu. 1999. New space vector modulation technique for inverter control. IEEE Power Electronics Specialists Conference. l.2: 777-782.

[3] J. S. Lai and F. Z. Peng. 1996. Multilevel convertersA new breed of power converters. IEEE Trans. Ind. Applicat. 32(May/June): 509-517.

[4] C. Hochgraf, R. Lasseter, D. Divan and T. A. Lipo. 1994. Comparison of multilevel inverters for static var compensation. In: Conf. Rec. IEEE-IAS Annu. Meeting. October. pp. 921-928.

[5] T. A. Meynard and H. Foch. 1992. Multi-level choppers for high voltage applications. Eur. Power Electron. Drives J. 2(1): 41.

[6] N. S. Choi, J. G. Cho and G. H. Cho. 1991. A general circuit topology of multilevel inverter. In: Proc. IEEE PESC'91. June. pp. 96-103.

[7] H.W. Van der Broeck, H.C. Skudelny and G.V.S tanke. 1988. Analysis and realization of a pulse-width modulator based on voltage space vectors. IEEE Transactions on Industry Applications. 24(1): 142150.

[8] Muhamed H. Rashid. Power Electronics Circuits, Devices and Applications.

[9] Jose Rodriguez, Jin-Sheng Lai and Fang Zheng Peng. 2002. Multilevel inverters: A survey of topologies, Control applications. IEEE Transactions on Industrial Electronics. 49(4): 724-738.

[10] F. Canales, P.M. Barbosa and F.C. Lee. 2000. A zero voltage and zero current switching three level dc-dc converter. In: Proc. of IEEE, APEC, New Orleans, LA. February. pp. 314-320.

[11] R. Radl, L. Balogh and N.O. Sokal. 1991. A novel soft switching full bridge DC-DC converter analysis, design considerations and experimental results at 1.5 KW, 100 kHz. IEEE transactions power electronics. 6: 408-418. July.

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