

## ANFIS Controller based Voltage Controlled DSTATCOM Using External Inductor

S. K. Sameer<sup>1</sup>, PG Scholar, Department of EEE, SHREE Institute of Technical Education, Gopalapuram, Tirupati, A.P, India

Y. Peraiyah<sup>2</sup>, M.Tech (PE), Department of EEE, SHREE Institute of Technical Education, Gopalapuram, Tirupati, A.P, India

**ABSTRACT**—this project proposes the Design of External Inductor for Improving Performance of DSTATCOM with ANFIS for better Voltage regulation & harmonic reduction. A DSTATCOM is used for load voltage regulation and its performance mostly is contingent upon the feeder impedance and its nature (resistive, inductive, stiff, non stiff). On the other hand, a study for investigating voltage regulation performance of DSTATCOM with ANFIS depending upon network parameters is not well defined. This paper aims to provide a comprehensive study of design, operation, and flexible ANFIS control of a DSTATCOM operating in voltage control mode. A detailed analysis of the voltage regulation capability of DSTATCOM under various feeder impedances is presented. Then, a benchmark design procedure to compute the value of external inductor is presented. A dynamic reference load voltage generation scheme is also developed, which allows DSTATCOM to compensate load reactive power during normal operation, in addition to providing voltage support during disturbances. Simulation results validate the effectiveness of the proposed ANFIS scheme.

**Index Terms**—Distribution static compensator (DSTATCOM), power factor, power quality (PQ), voltage control, ANFIS controller.

### I. INTRODUCTION

Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. The evolution of power electronic devices, nonlinear loads, and unbalanced loads has degraded the power quality in the power distribution network. The distribution static compensator is a shunt active filter, which injects currents into the point of common coupling (PCC) (the common point where load, source, and DSTATCOM are connected) such that the harmonic filtering, power factor correction, and load balancing can be achieved. In practice, the presence of feeder impedance and nonlinear loads distorts the terminal voltage (PCC) and source currents. The load compensation using state feedback control of DSTATCOM with shunt filter capacitor gives better results. The switching frequency components in the terminal voltages and source currents are eliminated by using state feedback control of shunt filter capacitor. In this situation, DSTATCOM should operate in CCM. However, due to grid faults, source voltage (stiff or non-stiff) can change at any time and then VCM operation is required. DSTATCOM regulates the load voltage by indirectly regulating the voltage across the feeder impedance. When a load is connected to nearly a stiff source, feeder impedance will be negligible. Faults in a widespread power system as well as switching of sizably voluminous loads engender voltage perturbances such as sag and swell in a distribution system. These power quality (PQ) quandaries significantly degrade the performance of sensitive loads like process-control industry, electronics equipment, adjustable drives, etc.

Power quality is one of the most consequential aspects concerned by utility and residential customer, especially when it becomes a very sensitive issue for industrial consumer. Power quality betokens the faculty to receive pristine electrical voltage sinusoidal waveform at distribution point. It is conspicuous that everyone will aim to gain the excellent quality in every situation no matter in which aspect, and power quality should not be omitted. Power quality quandaries are not incipient issues in a electrical power system and every electrical utilizer might want to minimize their effect on electrical equipment so that the highest possible power quality could be obtained by all of the users.

The transmutations of the voltage supplied even for very short period of time, which were not authentically mostly taken attention by public, is now very sumptuous due to their cause of infelicitous operation and shut down situation in manufacturing plants. For the purport of getting the highest efficiency in engenderment besides for sustaining of the most plausible operating cost, electrical customers were now agog for the high power quality. For instance, perturbances like voltage sag, which was introduced by the higher fault on the network, will influence more number of customer victims. Ergo, an opportune study and tenaciousness about the puissance quality perturbances should be conducted solemnly as well as the extenuation manners not only to consummate customers demand, but withal increase the reputation and quality of electrical power in our country.

In order to further understand the sophisticated power quality quandaries, the recordings of all perturbances are now done by installing the on-line power quality monitoring system. Besides that, sundry professional surveys had conducted in date. Hence, it is conspicuously that power quality perturbances are now became the very crucial topic for us to understand and study more. It signifies that the detection and mitigation of voltage sag in electrical power system are withal very paramount to achieve amelioration in power system so that their benefits could be experienced by people in whole country.

From decades to decades, power electronics have been introduced and developed further due to its economical and power preserving advantages. Flexible AC Transmission System (FACTS) are widely used to solve power quality perturbances and Distribution Static Compensator (DSTATCOM) is one of the members of FACTS contrivances family which is efficacious and flexible. Its function is akin to the utilization of synchronous transformer. In other words, DSTATCOM is an expeditious-respond reactive power source compensator, which can opportunely solve varies power perturbances with congruous controller designed, such as voltage sag, voltage swell, flicker, harmonic, and transient. It contains an injection transformer, a voltage source converter (VSC) and a PWM controller with concrete control scheme in order to perform its main function efficient and efficaciously. In this thesis, the function of DSTATCOM in voltage mitigation was mainly be discussed and it is one of the most paramount function of D-STATCOM contrivances.

Conventionally, static var compensator (SVC) is utilized to regulate load voltage, compensate reactive current, and amend transient stability. However, the SVC causes quandaries like harmonic current injection in the system, harmonic amplification, and possible resonance with the source impedance. Distribution static compensator (DSTATCOM) has been proposed to surmount the inhibitions of SVC [3]–[9]. A DSTATCOM is one of the most efficacious solutions to regulate the load voltage. It provides load voltage regulation by supplying fundamental reactive current into source.

However, most of the conventional DSTATCOMs utilized for voltage regulation consider highly inductive and/or significantly astronomically immense feeder impedance. This is conventionally erroneous in a distribution system where feeder impedance used to be resistive in nature. In this scenario, the DSTATCOM will have diminutive voltage regulation capability. Another consequential is-sue is the generation of reference load voltage. In conventional DSTATCOM application for voltage regulation, reference load voltage is set at 1.0 per unit (p.u.). At this load voltage, voltage-source inverter (VSI) always exchanges reactive power with the source with leading power factor. This causes continuous power losses in the feeder and VSI. Additionally, a conventional DSTATCOM requires high-current rating VSI to provide voltage support. This high-current requisite increases the potency rating of the VSI and engenders more losses in the switches as well as in the feeder.

The voltage regulation performance of DSTATCOM mainly depends upon the feeder impedance and its nature (resistive, inductive, stiff, and nonstiff). For voltage control mode (VCM) operation of DSTATCOM and/or grid-connected inverters, the conception of inserting an external inductor in line has been reported. However, in these schemes, only the concept has been introduced leaving ample scope for further investigation and insight into the design details.

The focus of this paper is to provide a detailed design procedure for culling the external inductor which satiates several practical constraints, sanction DSTATCOM to regulate load voltage in stiff as well as resistive feeder, reduce the current requisite for mitigation of sag, and reduce the system losses. With coordinated control of the load fundamental current, terminal voltage, and voltage across the external inductor, a dynamic reference load voltage generation scheme is presented. This scheme ascertains unity power factor (UPF) operation during mundane operation and maintains load voltage constant during voltage perturbances. Detailed simulation and experimental results are included to verify the DSTATCOM performance.

## II. DSTATCOM IN THE POWER DISTRIBUTION SYSTEM

Fig. 1 shows the power circuit diagram of the DSTATCOM topology connected in the distribution system.  $L_s$  and  $R_s$  are source inductance and resistance, respectively. An external inductance  $L_{ext}$  is included in series between load and source points. This inductor helps DSTATCOM to achieve load voltage regulation capability even in worst grid conditions, i.e., resistive or stiff grid. From IEEE-519 standard, point of commoncoupling (PCC) should be the point which is accessible to both the utility and the customer for direct measurement [20]. Therefore, the PCC is the point where  $L_{ext}$  is connected to the source. The DSTATCOM is connected at the point where load and

$L_{ext}$  are connected. The DSTATCOM uses a three-phase four-wire VSI. A passive LC filter is connected in each phase to filter out high-frequency switching components. Voltages across dc capacitors,  $V_{dc1}$  and  $V_{dc2}$ , are maintained at a reference value of  $V_{dcref}$ .

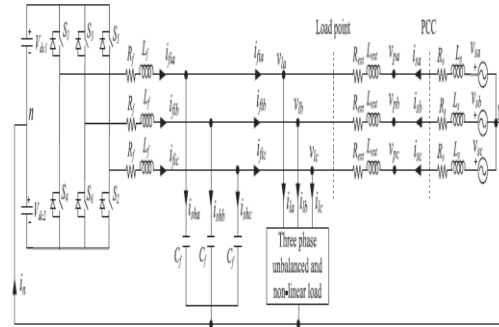


Fig. 1. Three-phase equivalent circuit of DSTATCOM topology in the distribution system

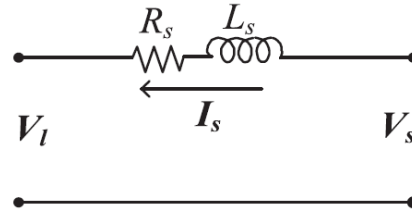


Fig. 2. Equivalent source-load model without considering external inductor.

## III. EFFECT OF FEEDER IMPEDANCE ON VOLTAGE REGULATION

To demonstrate the effect of feeder impedance on voltage regulation performance, an equivalent source-load model without considering external inductor is shown in Fig. 2. The current in the circuit is given as

$$I_s = \frac{V_s - V_l}{Z_s} \quad (1)$$

where  $V_s = V_s \angle \delta$ ,  $V_l = V_l \angle 0$ ,  $I_s = I_s \angle \phi$ , and  $Z_s = Z_s \angle \theta_s$ , with  $V_s$ ,  $V_l$ ,  $I_s$ ,  $Z_s$ ,  $\delta$ ,  $\phi$ , and  $\theta_s$  are rms source voltage, rms load voltage, rms source current, feeder impedance, load angle, power factor angle, and feeder impedance angle, respectively. The three-phase average load power ( $P_l$ ) is expressed as

$$P_l = \text{Real} [3 V_l I_s^*] \quad (2)$$

Substituting  $V_l$  and  $I_s$  into (2), the load active power is

$$P_l = \frac{3 V_l^2}{Z_s} \left[ \frac{V_s}{V_l} \cos(\theta_s - \delta) - \cos \theta_s \right] \quad (3)$$

Rearranging (3), expression for  $\delta$ s computed as follows:

$$\delta = \theta_s - \cos^{-1} \left[ \frac{V_l}{V_s} \left( \cos \theta_s + \frac{P_l Z_s}{3 V_l^2} \right) \right] \quad (4)$$

For power transfer from source to load with stable operation in an inductive feeder,  $\delta$  must be positive and less than  $90^\circ$ . Also, all the terms of the second part of (4), i.e., inside  $\cos^{-1}$ , are amplitude and will always be positive. Therefore, the value of the second part will be between "0" and " $\pi/2$ " for the entire operation of the load. Consequently, the load angle will lie between  $\theta$  and  $(\theta - \pi/2)$  under any load operation, and therefore, maximum possible load angle is  $\theta$ . The vector expression for source voltage is given as follows:

$$\mathbf{V}_s = V_l + I_s Z_s \angle (\theta_s + \phi) \quad (5)$$

A DSTATCOM regulates the load voltage by injecting fundamental reactive current. To demonstrate the DSTATCOM voltage regulation capability at different supply voltages for different  $R_s/X_s$  vector diagrams using (5) are drawn in Fig. 3. To draw these diagrams, load voltage  $V_l$  is taken as reference phasor having the nominal value  $OA$  (1.0 p.u.). With aim of making  $V = V_s = 1.0$  p.u., locus of  $V_s$  will be a semicircle of radius  $V$ . Since the maximum possible load angle is  $90^\circ$  in an inductive feeder, phasor  $V_s$  can be anywhere inside curve  $OACBO$ . It can be seen that the value of  $\theta_s + \phi$  must be greater than  $90^\circ$  for zero voltage regulation. Additionally, it is possible only when power factor is leading at the load terminal as  $\theta_s$  cannot be more than  $90^\circ$ .

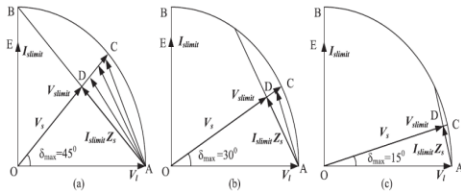


Fig. 3. Voltage regulation performance curve of DSTATCOM at different  $R_s/X_s$ . (a) For  $R_s/X_s = 1$ . (b) For  $R_s/X_s = \sqrt{3}$ . (c) For  $R_s/X_s = 3.73$

Fig. 3(a) shows the limiting case when  $R_s/X_s = 1$ , i.e.,  $\theta_s = 45^\circ$ . From (4), the maximum possible load angle is  $45^\circ$ . The maximum value of angle,  $\theta_s + \phi$ , can be  $135^\circ$  when  $\phi$  is  $90^\circ$ . Hence, the limiting source current phasor  $OE$ , which is denoted by  $I_{s\text{limit}}$ , will lead the load voltage by  $90^\circ$ . Lines  $OC$  and  $AB$  show the limiting vectors of  $V_s$  and  $I_s Z_s$ , respectively, with  $D$  as the intersection point. Hence, area under  $ACDA$  shows the operating region of DSTATCOM for voltage regulation. The point  $D$  has a limiting value of  $V_{\text{limit}} = I_s Z_s = 0.706$  p.u. Therefore, maximum possible voltage regulation is 29.4%. However, it is impossible to achieve these two limits simultaneously as  $\delta$  and  $\phi$  cannot be maximum at the same time. Again if  $Z_s$  is low, the source current, which will be almost inductive, will be enough to be realized by the DSTATCOM.

Fig. 3(b) considers case when  $R_s/X_s = \sqrt{3}$ , i.e.,  $\theta_s = 30^\circ$ . The area under  $ACDA$  shrinks, which shows that with the increase in  $R_s/X_s$  from the limiting value, the voltage regulation capability decreases. In this case, the limiting values of  $V_{\text{limit}}$  and  $I_s Z_s$  are found to be 0.866 and 0.5 p.u., respectively. Here, maximum possible voltage regulation is 13.4%. However, due to high-current requirement; a practical DSTATCOM can provide very small voltage regulation.

Voltage regulation performance curves for more resistive grid, i.e.,  $\theta_s = 15^\circ$ , as shown in Fig. 3(c), can be drawn similarly. Here, area under  $ACDA$  is negligible. For this case, hardly any voltage regulation is possible. Therefore, more the feeder is resistive in nature,

lesser will be the voltage regulation capability. Therefore, it is inferred that the voltage regulation capability of DSTATCOM in a distribution system mainly depends upon the feeder impedance. Due to resistive nature of feeder in a distribution system, DSTATCOM voltage regulation capability is limited. Moreover, very high current is required to mitigate small voltage disturbances, which results in higher rating of insulated-gate bipolar transistor switches as well as increased losses. One more point worth to be noted is that, in the resistive feeder, there will be some voltage drop in the line at nominal source voltage which the DSTATCOM may not be able to compensate to maintain load voltage at 1.0 p.u. even with an ideal VSI.

#### IV. SELECTION OF EXTERNAL INDUCTOR FOR VOLTAGE REGULATION IMPROVEMENT AND RATING REDUCTION

This section presents a generalized procedure to select external inductor for improvement in DSTATCOM voltage regulation capability while reducing the current rating of VSI. Fig. 4 shows single-phase equivalent DSTATCOM circuit diagram in distribution system. With balanced voltages, source current will be

$$I_s = \frac{V_s \angle \delta - V_l \angle 0}{(R_s + R_{\text{ext}}) + j(X_s + X_{\text{ext}})} = \frac{V_s \angle \delta - V_l \angle 0}{R_{\text{sef}} + jX_{\text{sef}}} \quad (6)$$

where  $R_{\text{sef}} = R_s + R_{\text{ext}}$  and  $X_{\text{sef}} = X_s + X_{\text{ext}}$  are effective feeder resistance and reactance, respectively.  $R_{\text{ext}}$  is equivalent series resistance (ESR) of external inductor, and will be small. With  $\theta_{\text{sef}} = \tan^{-1} X_{\text{sef}}/R_{\text{sef}}$  and  $Z_{\text{sef}} = \sqrt{R_{\text{sef}}^2 + X_{\text{sef}}^2}$  as effective impedance angle and effective feeder impedance, respectively, the imaginary component of  $I_s$  is given as

$$I_s^{\text{im}} = \frac{V_l \sin \theta_{\text{sef}} + V_s \sin(\delta - \theta_{\text{sef}})}{Z_{\text{sef}}} \quad (7)$$

With the addition of external impedance, the effective feeder impedance becomes predominantly inductive. Hence,  $Z_{\text{sef}} \approx X_{\text{sef}}$ . Therefore, approximated  $I_s^{\text{im}}$  will be

$$I_s^{\text{im}} = \frac{V_l \sin \theta_{\text{sef}} + V_s \sin(\delta - \theta_{\text{sef}})}{X_{\text{sef}}} \quad (8)$$

DSTATCOM Power rating ( $S_{\text{vsi}}$ ) is given as follows [21]:

$$S_{\text{vsi}} = \sqrt{3} \frac{V_{\text{dc}}}{\sqrt{2}} I_{\text{vsi}} \quad (9)$$

Where  $I_{\text{vsi}}$  is the rms phase current rating of the VSI and  $V_{\text{dc}}$  is the voltage maintained at the dc capacitors. The DSTATCOM aims to inject harmonic and reactive current component of load currents. Suppose  $I_{\text{lim}}$  is the maximum rms reactive and harmonic current rating of the load; then, the value of compensator current used for voltage regulation (same as  $I_{\text{lim}}$ ) is obtained by subtracting  $I_{\text{lim}}$  from  $I_{\text{vsi}}$  and given as follows:

$$I = I_{\text{vsi}} - I_{\text{lim}}^{\text{im}} = \frac{\sqrt{2} S_{\text{vsi}}}{\sqrt{3} V_{\text{dc}}} - I_{\text{lim}}^{\text{im}} \quad (10)$$

Comparing (8) and (10) while using the value of  $\delta$  from (4), the following expression is obtained:

$$X_{\text{sef}} = \frac{V_l \sin \theta_{\text{sef}} - V_s \sin \left[ \cos^{-1} \left[ \frac{V_l}{V_s} \left( \cos \theta_{\text{sef}} + \frac{P_l X_{\text{sef}}}{3 V_{\text{dc}}^2} \right) \right] \right]}{\frac{\sqrt{2} S_{\text{vsi}}}{\sqrt{3} V_{\text{dc}}} - I_{\text{lim}}^{\text{im}}} \quad (11)$$

The above expression is used to compute the value of external inductor. A design example of external inductor, used for this study, is given in the next section.

### V. DESIGN EXAMPLE OF EXTERNAL INDUCTOR

Here, it is assumed that the considered DSTATCOM protects load from a voltage sag of 60%. Hence, source voltage  $V_s=0.6$  p.u. is considered as worst case voltage disturbances. During voltage disturbances, the loads should remain operational while improving the DSTATCOM capability to mitigate the sag. Therefore, the load voltage during voltage sag is maintained at 0.9 p.u., which is sufficient for satisfactory operation of the load. In the present case, maximum required value of  $I^{lim}$  is 10 A. With the system parameters given in Table I, the effective reactance after solving (11) is found to be  $2.2 \Omega$  ( $L_{ser} = 7$  mH). Hence, value of external inductance,  $L_{ext}$ , will be 6.7 mH.

This external inductor is selected while satisfying the constraints such as maximum load power demand, rating of DSTATCOM, and amount of sag to be mitigated. In this design example, for base voltage and base power rating of 400 V and 10 kVA, respectively, the value of external inductance is 0.13 p.u. Moreover, with a total inductance of 7 mH (external and actual grid inductance), the total impedance will be 0.137 p.u. The short-circuit capacity of the line will be  $1/0.13 = 7.7$  p.u., which is sufficient for the satisfactory operation of the system. Additionally, a designer always has flexibility to find suitable value of  $L_{ext}$  if the constraints are modified or circuit conditions are changed. Moreover, the conventional DSTATCOM operated for achieving voltage regulation uses large feeder inductances [11], [13].

TABLE I

SIMULATION PARAMETERS

System quantities	Values
Source voltage	230 V rms L-N (1.0 p.u.), 50 Hz
Feeder impedance	$R_s = 0.3 \Omega, L_s = 0.3$ mH, $R_s / X_s = 3.185$
External impedance	$L_{ext} = 6.7$ mH, $R_{ext} = 0.07 \Omega$
Linear load	$Z_{1a} = 30 + j62.8 \Omega, Z_{1b} = 40 + j78.5 \Omega,$ $Z_{1c} = 50 + j50.24 \Omega$
Nonlinear load	Three-phase rectifier supplying RL load of 50 $\Omega$ and 200 mH
VSI parameters	$V_{dc} = 520$ V, $C_{dc} = 2600 \mu$ F, $L_f = 5$ mH, $C_f = 20 \mu$ F, $S_{vsi} = 30$ kVA
PI gains	$K_{p\delta} = 8.5 e^{-7}, K_{i\delta} = 1.8 e^{-6}$

With the external inductance while neglecting its ESR,  $R_s/X_{ser}$  will be 0.13, i.e.,  $\theta_{ser} = 83^\circ$ . Voltage regulation performance curves of the DSTATCOM in this case are shown in Fig. 5, of the stable operating range  $OABO$ . Hence, introduction of external inductor greatly improves the DSTATCOM voltage regulation capability. Additionally, due to increased effective feeder impedance, the current requirement for sag mitigation also reduces. Moreover, if ESR of the external inductor is included, then the equivalent feeder impedance angle changes slightly (i.e., from  $83^\circ$  to  $80.45^\circ$ ) and has negligible effect on the expression obtained in (11) as well as the voltage regulation capability of the DSTATCOM.

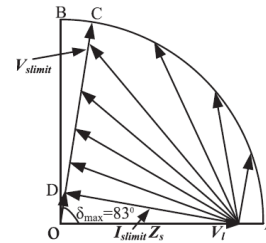


Fig. 4. Voltage regulation performance of DSTATCOM with external inductance.

### VI. DESIGN OF ADAPTIVE NEURO-FUZZY CONTROLLER

Adaptive neuro fuzzy inference system (ANFIS) integrates the best features of fuzzy systems and neural networks, and it has potential to capture the benefits of both in a single framework. ANFIS is a kind of artificial neural network that is based on Takagi-sugeno fuzzy inference system, which is having one input and one output. Using a given data set, the toolbox function of ANFIS constructs a fuzzy inference system (FIS) where the membership function parameters are tuned (adjusted) using a back propagation algorithm. In order to have an idea of optimized ANFIS architecture for proposed control, an initial data is generated from normal PI regulator and the data is saved in workspace of MATLAB. Then the ANFIS command window is opened by typing anfis editor in the main MATLAB window. Then the data previously saved in workspace is loaded in the ANFIS command window to generate an optimized ANFIS architecture as shown in Fig. 3.

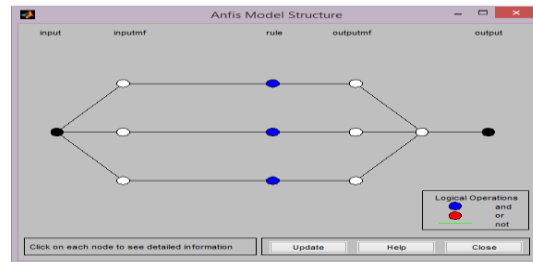


Figure. 4(a) Optimized ANFIS architecture suggested by MATLAB/anfiseditor.

In Fig. 4 shows schematic of the proposed ANFIS based control architecture. The node functions of each layer in the ANFIS architecture are described as follows:

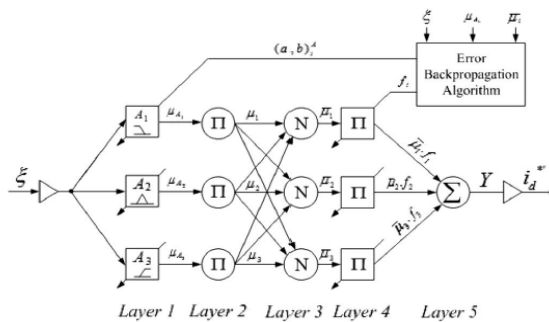


Figure. 5 Schematic of the proposed ANFIS-based control architecture.

The error between reference dc-link voltage and actual dc-link voltage ( $\xi = V_{dc}^* - V_{dc}$ ) is given to the neuro-fuzzy controller and the same error is used to tune the precondition and consequent parameters [10]. The control of dc-link voltage gives the active power current component ( $i_d^*$ ), which is further modified to take in account of active current component injected from RES ( $i_{Rcm}$ ). The node functions of each layer in ANFIS architecture are as described below:

**Layer 1:** This layer is also known as fuzzification layer where each node is represented by square. Here, three membership functions are assigned to each input. The trapezoidal and triangular membership functions are used to reduce the computation burden as shown in Fig. 5. And the corresponding node equations are as given below:

$$\mu_{A1}(\varepsilon) = \begin{cases} 1 & \varepsilon \leq b_1 \\ \frac{\varepsilon - a_1}{b_1 - a_1} & b_1 < \varepsilon < a_1 \\ 0 & \varepsilon \geq a_1 \end{cases}$$

$$\mu_{A2}(\varepsilon) = \begin{cases} 1 - \frac{\varepsilon - a_1}{0.5b_2} & |\varepsilon - a_2| \leq 0.5b_2 \\ 0 & |\varepsilon - a_2| \geq 0.5b_2 \end{cases}$$

$$\mu_{A3}(\varepsilon) = \begin{cases} 0 & \varepsilon \leq a_3 \\ \frac{\varepsilon - a_1}{b_1 - a_1} & a_3 < \varepsilon < b_3 \\ 1 & \varepsilon \geq b_3 \end{cases} \quad (12)$$

where the value of parameters ( $a_i, b_i$ ) changes with the change in error and accordingly generates the linguistic value of each membership function. Parameters in this layer are referred as premise parameters or precondition parameters.

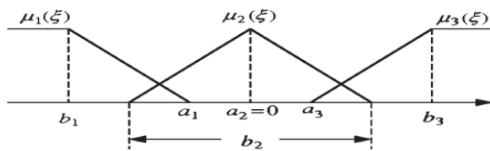


Figure. (6a) Fuzzy membership functions.

**Layer 2:** Every node in this layer is a circle labelled as  $\Pi$ , which multiplies the incoming signals and forwards it to next layer

$\mu_i = \mu_{A_i}(\varepsilon_1) \cdot \mu_{B_i}(\varepsilon_2) \dots i=1,2,3, \dots$  But in our case there is only one input, so this layer can be ignored and the output of first layer will directly pass to the third layer. Here, the output of each node represents the firing strength of a rule.

**Layer 3:** Every node in this layer is represented as circle. This layer calculates the normalized firing strength of each rule as given below:

$$\bar{\mu}_i = \frac{\mu_i}{\mu_1 + \mu_2 + \mu_3} \quad (13)$$

**Layer 4:** Every node in this layer is a node function

$$O_i = \bar{\mu}_i \cdot f_i = \bar{\mu}_i (a_0^i + a_1^i \varepsilon) \quad i=1,2,3.$$

where the parameters ( $a_0^i, a_1^i$ ) are tuned as the function of input ( $\xi$ ). The parameters in this layer are also referred as consequent parameters.

**Layer 5:** This layer is also called output layer which computes the output as given below: The output from this layer is multiplied with the normalizing factor to obtain the active power current component.

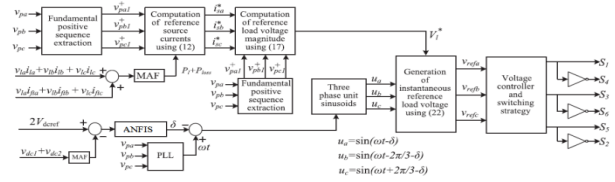


Fig. 6. Block diagram of the proposed flexible control strategy.

$$P_{\text{loss}} = \frac{1}{T} \int_{t_1-T}^{t_1} (v_{la} i_{fta} + v_{lb} i_{ftb} + v_{lc} i_{fte}) dt. \quad (14)$$

The reference source currents must be in phase with the respective fundamental positive-sequence PCC voltages for achieving UPF at the PCC. Instantaneous PCC voltage and reference source current in phase- $a$  can be defined as follows:

$$v_{pa1}^+ = \sqrt{2} V_{pa1}^+ \sin(\omega t - \varphi_{pa1}^+), \quad i_{sa}^* = \sqrt{2} I_{sa}^* \sin(\omega t - \varphi_{pa1}^+) \quad (15)$$

where  $V_{pa1}^+$  and  $\varphi_{pa1}^+$  are rms voltage and angle of fundamental positive-sequence voltage in phase- $a$ , respectively.  $I_{sa}^*$  is the rms reference source current obtained from (12). With external impedance, the expected load voltage is given as follows:

$$V_{la} = V_{pa1}^+ - I_{sa}^* Z_{\text{ext}}. \quad (16)$$

From (15) and (16), the load voltage magnitude will be

$$V_{la} = \sqrt{\left[ (V_{pa1}^+ \cos \varphi_{pa1}^+ - I_{sa}^* Z_{\text{ext}} \cos(\theta_{\text{ext}} - \varphi_{pa1}^+))^2 + (V_{pa1}^+ \sin \varphi_{pa1}^+ - I_{sa}^* Z_{\text{ext}} \sin(\theta_{\text{ext}} - \varphi_{pa1}^+))^2 \right]}. \quad (17)$$

With UPF at the PCC, the voltage across the external inductor will lead the PCC voltage by  $90^\circ$ . Neglecting ESR of external inductor, it can be observed that the voltage across external inductor improves the load voltage compared to the PCC voltage.

This highlights another advantage of external inductor where it helps in improving the load voltage. As long as  $V_{la}$  lies between 0.9 and 1.1 p.u., same voltage is used as reference terminal voltage ( $V^*/I$ ), i.e.,

$$\text{if } V_{la} \in [0.9 - 1.1 \text{ p.u.}], \text{ then } V_l^* = V_{la}. \quad (18)$$

2) Operation During Sag: Voltage sag is considered when value of (18) is less than 0.9 p.u. To keep filter current minimum, the reference voltage is set to 0.9 p.u. Therefore,

$$V_l^* = 0.9 \text{ p.u.} \quad (19)$$

3) Operation During Swell: A voltage swell is considered when any of the PCC phase voltage exceeds 1.1 p.u. In this case, reference load voltage ( $V^*/I$ ) is set to 1.1 p.u., which results in minimum current injection. Therefore,

$$V_l^* = 1.1 \text{ p.u.} \quad (20)$$

B. Computation of Load Angle ( $\delta$ )

Average real power at the PCC ( $P_{pcc}$ ) is sum of average load power ( $P_l$ ) and VSI losses ( $P_{loss}$ ). The real power  $P_{pcc}$  is taken from the source depending upon the angle between source and load voltages, i.e., load angle  $\delta$ . If DST AT COM dc bus capacitor voltage is regulated to a reference value, then in steady-state condition,  $P_{loss}$  is a constant value and forms a fraction of  $P_{pcc}$ . Consequently,  $\delta$  is also a constant value.

The dc-link voltage is regulated by generating a suitable value of  $\delta$ . The average voltage across dc capacitors ( $V_{dc1} + V_{dc2}$ ) is compared with a reference voltage and error is passed through a PI controller. Output of PI controller,  $\delta$ , is given as

$$\delta = K_p \delta e_{vdc} + K_i \int e_{vdc} dt \quad (21)$$

Where  $v_{dc} = 2 V_{dcref} - (V_{dc1} + V_{dc2})$  is the voltage error.  $K_p \delta$  and  $K_i \delta$  are proportional and integral gains, respectively.

### C. Generation of Instantaneous Reference Voltage

Selecting suitable reference load voltage magnitude and computing load angle  $\delta$  from (21), the three-phase balanced sinusoidal reference load voltages are given as follows:

$$\begin{aligned} v_{refa} &= \sqrt{2} V_l^* \sin(\omega t - \delta) \\ v_{refb} &= \sqrt{2} V_l^* \sin(\omega t - 2\pi/3 - \delta) \\ v_{refc} &= \sqrt{2} V_l^* \sin(\omega t + 2\pi/3 - \delta). \end{aligned} \quad (22)$$

These voltages are realized by the VSI using a predictive voltage controller [23].

## VII. MATLAB/SIMULINK RESULTS

The control scheme is implemented using PSCAD software. Simulation parameters are given in Table I. Fig 7(a) show the MATLAB/SIMULINK Model of the Proposed ANFIS based DST AT COM. Fig. 7(b) shows the Terminal voltages and source currents before compensation are plotted. Distorted and unbalanced source currents flowing through the feeder make terminal voltages unbalanced and distorted. Three conditions, namely, nominal operation, operation during sag, and operation during load change are compared between the traditional and proposed method. In the traditional method, the reference voltage is 1.0 p.u. whereas in the proposed method used to find the reference voltage.

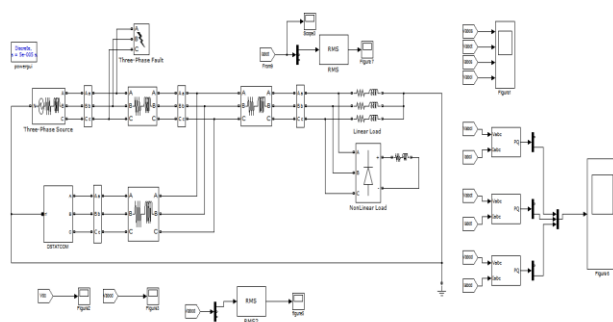
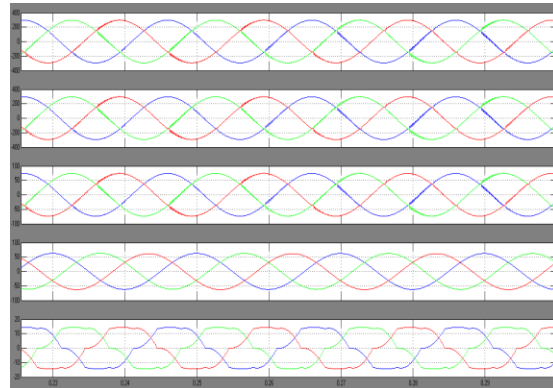


Fig 7(a)



(b)

Fig. 7(a) Simulink model of the proposed ANFIS based DST AT COM (b) PCC voltages, Load Voltages, Source currents & Filter Currents Load Currents using the traditional method.

### A. Nominal Operation

Initially, the traditional method is considered. Fig. 7(b),(a)–(c) shows the regulated terminal voltages and corresponding source currents in phases. These waveforms are balanced and sinusoidal. However, source currents lead respective terminal voltages which show that the compensator supplies reactive current to the source to overcome feeder drop, in addition to supplying load reactive and harmonic currents. Fig. 9

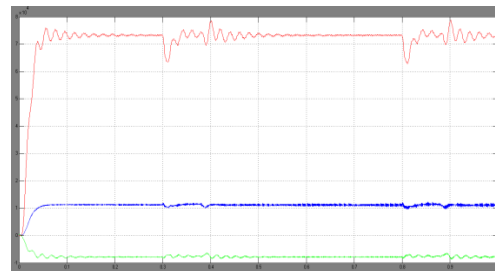


Fig 8 Reactive power of the Load , PCC & DSATCOM

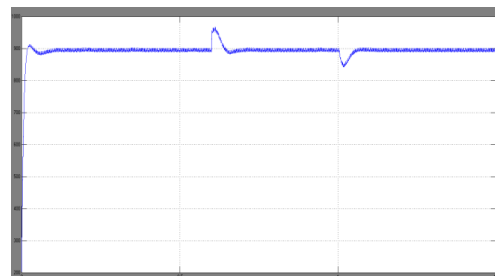


Fig. 9. (a) Voltage at the dc bus.

shows the dc bus voltage regulated at a nominal voltage of 1300 V. Fig. 9 shows the load angle settled around  $8.50^\circ$ . Using the proposed method, terminal voltages and source currents in phases,  $v_a$  and  $i_a$  are shown in Fig. 10(a)–(c), respectively. It can be seen that the respective terminal voltages and source currents are in phase with each other, in addition to being balanced and sinusoidal. Therefore, UPF is achieved

at the load terminal. For the considered system, waveforms of load reactive power (Ql), compensator reactive power (Qc), and reactive power at the PCC (Qpcc) in the traditional and proposed

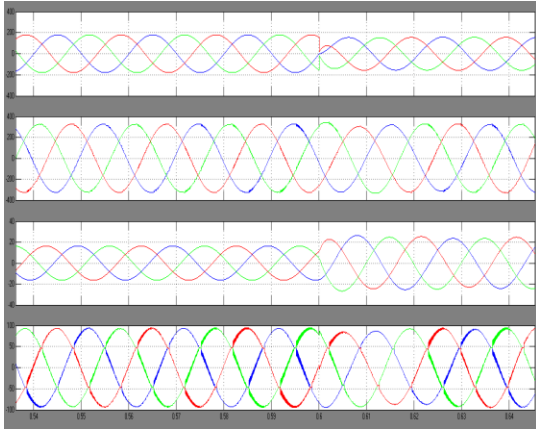


Fig. 10. Terminal voltages and source currents using the proposed method.

In the traditional method, the compensator needs to overcome voltage drop across the feeder by supplying reactive power into the source. As shown in Fig.8, reactive power that is supplied by the compensator and has a value of 4.7 kVAR is significantly more than the load reactive power demand of 2.8 kVAR. This additional reactive power of 1.9 kVAR goes into the source.

This confirms that significant reactive current flows along the feeder in the traditional method. However, in the proposed method, UPF is achieved at the PCC by maintaining suitable voltage magnitude. Thus, the reactive power supplied by the compensator is the same as that of the load reactive power demand. Consequently, reactive power exchanged by the source at the PCC is zero. Fig. 11 shows the source rms currents in phase for the traditional and proposed methods, respectively. The source current has decreased from 11.35 to 10.5 A in the proposed method. Consequently, it reduces the ohmic losses in the feeder.

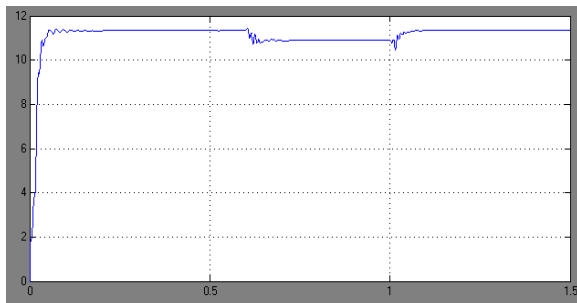
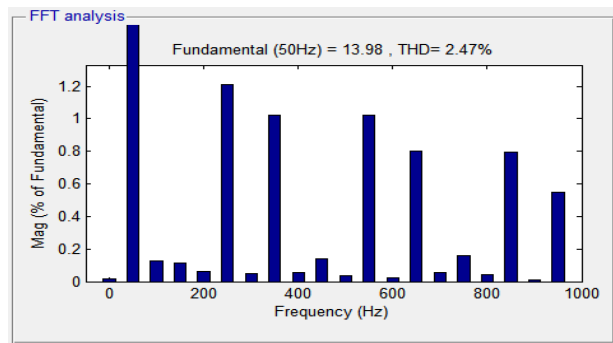


Fig. 11. Phase- source rms currents Proposed method.

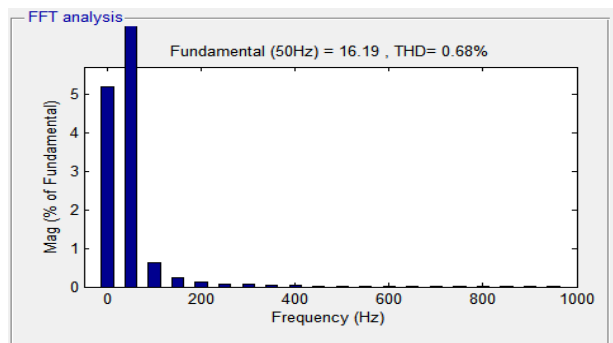
Fig. 11 shows the compensator rms currents in phase- for the traditional and proposed methods, respectively. The current has decreased from 8.4 to 5.2 A in Voltage at the dc bus and Compensator rms current in the proposed method. Fig 12 shows Source voltages, terminal voltages, voltage at dc bus and compensator rms current in proposed method.



Fig12 (a) Source voltages. (b) Terminal voltages. (c) Voltage at the dc bus. (d) Compensator rms current in the proposed method.



(a)



(b)

Fig 13 THD values of the Source Currents using (a) Traditional Method (b)Proposed ANFIS based DATCTOM

Fig 13. (a), (b) shows THD values of the source currents using a traditional method and proposed method i.e. ANFIS based controller. In traditional method THD values of the source currents showing 2.47%, in proposed method by using ANFIS based controller THD values of the source currents is 0.68%. So by using ANFIS based controller the total harmonic distortion will be reduced and it smoothens the waveforms by reducing harmonics.

## VIII CONCLUSION

This paper proposes another calculation to create reference voltage for a Distributed static compensator (DSTATCOM) with ANFIS Controller working in voltage control mode. The proposed plan displays a few points of interest contrasted with customary ANFIS controller based DSTATCOM where the reference voltage is subjectively taken as 1.0 p.u. The proposed ANFIS controller guarantees that Unity Power Factor (UPF) is accomplished at the heap terminal along with superficial operation, which is unrealistic in the conventional strategy. Likewise, the compensator infuses lower harmonics and, subsequently, lessens misfortunes in the feeder and voltage-source inverter. Further, a sparing in the rating of DSTATCOM is accomplished which expands its ability to moderate voltage list. About UPF is kept up, while managing voltage at the heap terminal, amid burden change. With these elements, this plan permits DSTATCOM with ANFIS Controller to handle power quality issues, consonant power, Voltage adjusting, and voltage regulation taking into account the heap prerequisite. Reproduction and MATLAB/SIMULINK results are introduced to exhibit the adequacy of the proposed ANFIS Controller.

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**Mr. S.K. Sameer is Completed** his B.Tech in Department of **EEE** in Siddharth institute of engg. and technology in 2013 and now pursuing his Master of Technology in Power Systems, EEE Department, SHREE Institute Technical Education, Gopalapuram, Tirupati, Andhra Pradesh, India. Interests in Power Generation, Distribution and Transmission.

**Mr. Y. Peraiah** is currently working as an Assistant Professor in EEE department in SHREE Institute of Technical Education, Gopalapuram, Tirupati, and Andhra Pradesh, India.