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# High Efficiency Single Phase Transformerless Inverter For Grid Connected Pv System

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**Abstract**

*The grid tied photovoltaic system suffers a great loss because the performance of the transformer present in the inverter. The cost of the transformer is high and the maintaince cost is also high. Therefore transformer less inverter are widely used in grid tied photovoltaic system, due to the benefits of achieving high efficiency and low cost. The sinusoidal pulse width modulation of full bridge transformer less inverters can achieve high efficiency by using metal oxide semiconductor field effect transistor. Various topology has been implemented for transformer less inverter, but in that there is a problem of loss and reverse recovery characteristics. In our paper we are going to implement the centre tapped H bridge transformer less inverter topology for grid tied photovoltaic system to avoid the losses and leakage current. A clamped branch is added in the transformer less inverter. The added clamping branch clamps the freewheeling voltage at the freewheeling period. As the common mode voltage is kept constant for the whole grid period that reduces the leakage current. The splitting structure of inductor at the region of grid side avoids reverse recovery voltage and this improves the efficiency of the system. The detailed analysis of our topology with the operational modes, leakage current analysis and design consideration were implemented.*

## I. INTRODUCTION

Transformer less inverters are widely used in grid-tied photovoltaic (PV) generation systems, due to the benefits of achieving high efficiency and low cost. Various transformer less inverter topologies have been proposed to meet the safety requirement of leakage currents, when no transformer is used in a grid connected photovoltaic system, a galvanic connection between the grid and PV array exists. In these conditions, dangerous leakage currents (common-mode currents) can appear through the stray capacitance between the PV array and the ground. In order to avoid these leakage currents, different inverter topologies that generate no varying common-mode voltages have been proposed

## II. VARIOUS TRANSFORMERLESS TOPOLOGIES

In recent years, there have been quite a few new transformerless PV inverters topologies, which eliminate traditional line frequency transformers to achieve lower cost and higher efficiency, and maintain lower leakage current as well. One unipolar inverter topology, H5, as shown in Fig.1, solves the ground leakage current issue and uses hybrid MOSFET and IGBT devices to achieve high efficiency.

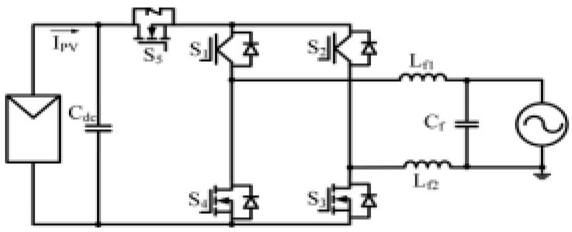


Fig.1. H5 Topology

This topology has high conduction losses due to the fact that the current must conduct through three switches in series during the active phase. Another disadvantage of the H5 is that the line-frequency switches S1 and S2 cannot utilize MOSFET devices because of the MOSFET body diode's slow reverse recovery. The slow reverse recovery of the MOSFET body diode can induce large turn-on losses, has a higher possibility of damage to the devices and leads to EMI problems. Shoot-through

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issues associated with traditional full bridge PWM inverters remain in the H5 topology due to the fact that the three active switches are series-connected to the dc bus.

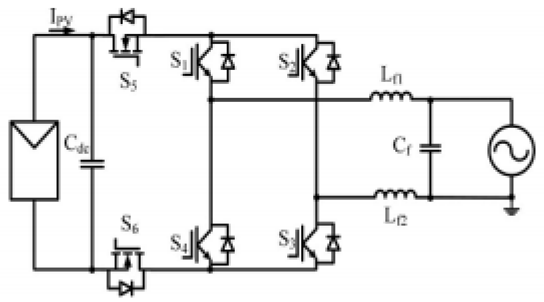


Fig.2. H6 Topology

H6 Topology uses MOSFETs to decrease the conduction loss of IGBTs in H5 topology, by splitting S5 of H5 topology into two MOSFETs i.e. S5 and S6 in series and operates them in high-frequency switching, S1−S4 in line grid line frequency switching. Uency switching, S1−S4 in line grid line frequency switching. Drawbacks of this inverter are higher conduction loss from four devices in conduction loop

## III.PROPOSED TOPOLOGY

The family of the proposed transformer less PV inverter topology is depicted in Fig. 3 which is derived according to the derivation method described in the prior section, where S1, S2, S4, and S5 are high-frequency switches, and S3 and S6 are low frequency freewheeling switches. The unidirectional clamping branch is constructed using switch S7 and diode D3 with a capacitor divider (Cdc1 and Cdc2) which clamps the CM voltage at the midpoint of dc link. LA,LB , and Co make up the LC type filter connected to the grid and Vpv represent the input dc voltage. The unipolar SPWM can be employed to the proposed topology with three-level output voltage. The MOSFET power switches are utilized as no reverse-recovery issues are required for the proposed configuration of the inverter for unity power factor operation. Consequently, the efficiency of the entire PV system is increased.

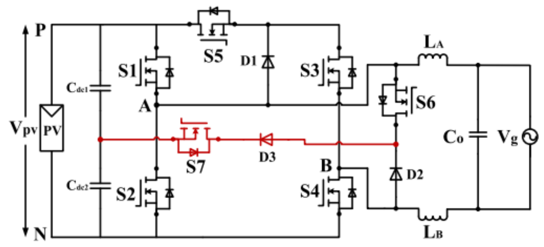


Fig 3 proposed transformer less grid-connected PV inverter structure

### 3.1 Operating principle

In order to analyse and verify, the circuit structure (a) is taken as an example, it shows the switching pattern for unity power factor operation, where the G1, G2, G3, G4, G5, G6 and G7 are the gate signals of the switches S1, S2, S3, S4, S5, S6 and S7. As can be seen, (S1, S4) and (S2, S5) commutate at the switching frequency with the identical commutation order in the positive and negative half cycle of the grid current, respectively. The operating principles of the proposed topology are shown. Four operation modes are proposed to generate the output voltage stste of +Vpv, 0 and –Vpv, which can explained as follows

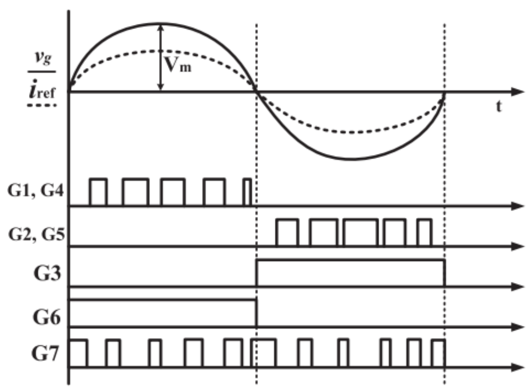


Fig 4 Gate drive signals of the proposed topology

1) Mode 1 is the active in the positive half cycle of the grid current.When S1,S4 are turned-on, the inductor current iL increases linearly through grid. In this mode, VAN = VPV and VBN = 0, thus VAB =VPV and the inductor current: **i t = Vpv−Vg/ L (t)**

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2) Mode 2 is the freewheeling mode in the positive half cycle of the grid current. The inductor current iL flows though S6 and D2, and reduces linearly under the effect of grid voltage. In this state, VAN falls and VBN rises unti their values are equal. If the voltages (VAN≈ VBN) are higher than half of the dc link voltage, freewheeling current flows through S7 & D3 to the midpoint of the dc link, results VAN and VBN are clamped at VPV/2. Therefore , at mode 2, VAN = VPV/2, VBN = VPV/2, the inverter output voltage VAB = 0 and the inductor current: $\mathbf{i\ t} = -\mathbf{Vg/\ L\ (t)}$

3) Mode 3 is the active mode in the negative half cycle of grid current. Similar to mode 1, when S2, S3, and S5 are turned-on, the voltage VAN = 0 and VBN = VPV, thus VAB = -VPV and the inductor current: $\mathbf{i\ t} = \mathbf{Vpv-Vg/\ L\ (t)}$

4) Mode 4 is the freewheeling mode in the negative half cycle of grid current. When S5 and S2 are turned-off, the inductor current flows throgh S3 and D1. Similar to mode 2, if the voltages ( VAN = VBN) are higher than half of the dc link voltag, freewheeling current flows through S7 and D3 to the mid-point of the dc link, results the voltages VAN and VBN are clamped at VPV/2. Therefore, in this mode, VAB = 0, and the inductor current: $\mathbf{i\ t} = -\mathbf{Vg/L\ (t)}$ As described above, the freewheeling path potential is clamped at the mid-point of the dc link during freewheeling period of positive and negative half cycle. As a result, the seen that the anti-parallel diodes of the MOSFETs remained inactive during the whole grid operation period. Therefore, the proposed could be implemented utilizing MOSFET switches. However, the body-diode will be activated if a phase shift is occurred in the inverter output voltage and current. Accordingly, the dependability of the system will be reduced becauce of the MOSFET anti-parallel diode low reverse recovery issues.

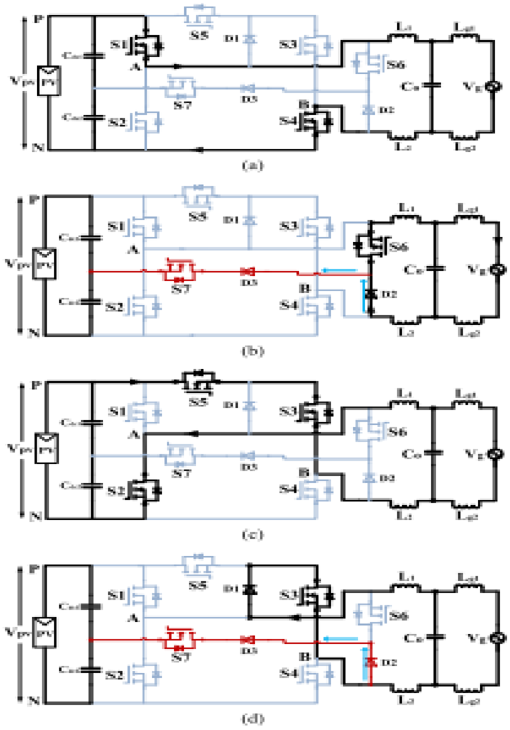


Fig. 5. Operating principle of the proposed topology: (a) Active and (b) freewheeling modes in the positive half cycle of the grid current, (c) active and (d) freewheeling modes in the negative half cycle of the grid curren

## IV.SIMULATION RESULTS

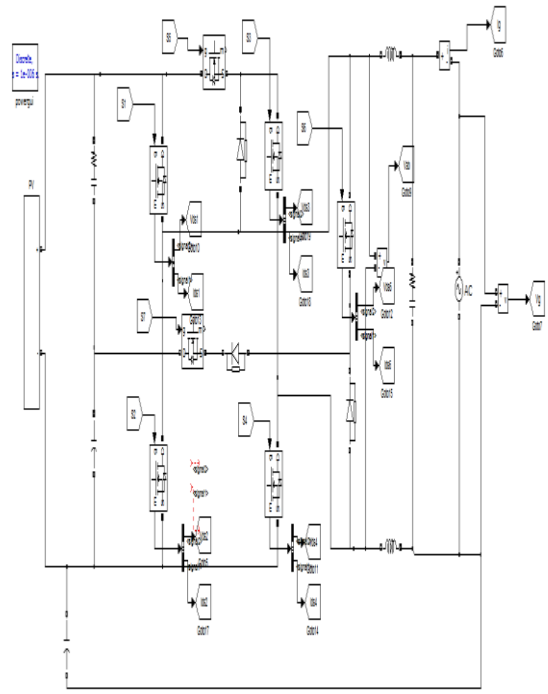

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Figure 6: Simulink model of proposed system

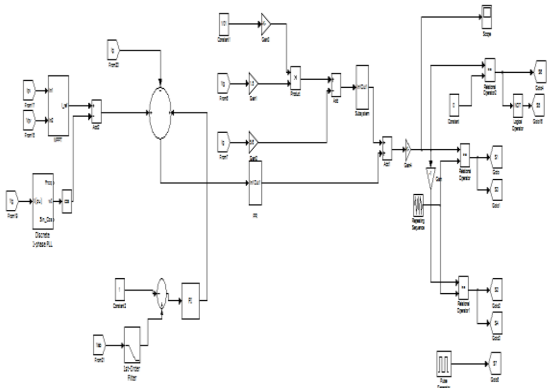

Figure 7: control diagram of proposed system

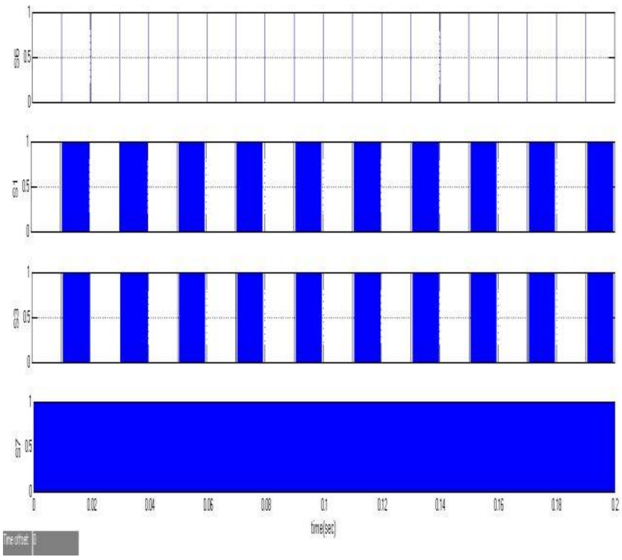

Figure 8 : Gates pulses of switches S6, S1, S3 and S7

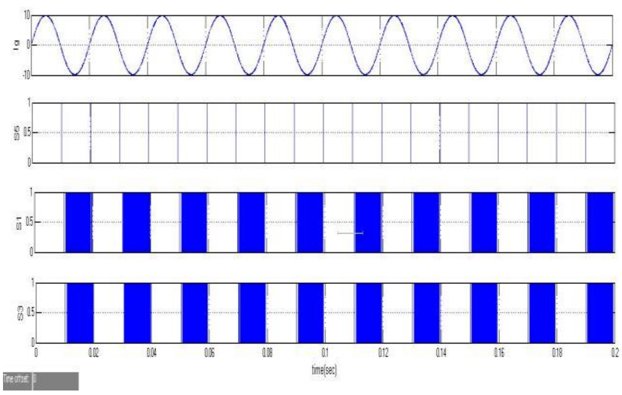

Figure 9 : Grid current(Ig) and gate pulses for switches S6, S1 and S3

In order to verify the performance of the proposed topology and to compare with other topologies, The Simulink model of proposed model is given in Figure 6 and It is clear that the gate signals are in agreement with the theoretical and the gate drive voltages are kept constant at the desired level. It also can be observed from Figure 8 and Figure 9 that the gate signals G1 and G4 are well synchronized, while G7 is the contrary gate pulse of G1 and G4 with a small dead band.

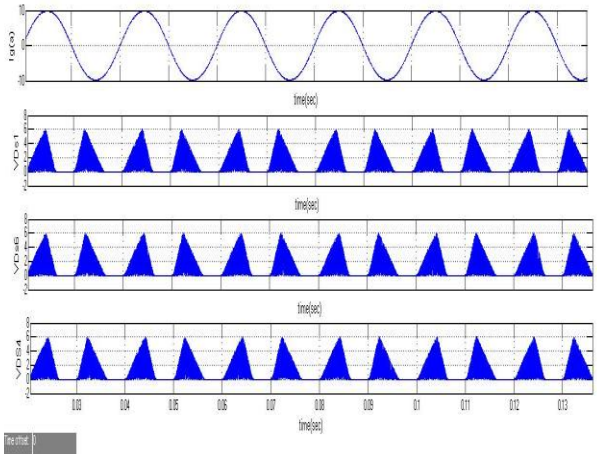

Figure 10: Drain to source voltage of different switches S1, S6 and S4

Figure 10 shows the drain-source voltage waveforms of the switches S1, S4, and S6. This shows that the switching voltages of the switches are half of the dc input voltage without any overstress. The partial expansion of Figure 8 is showing that the switches S1 and S4 almost share the dc-link voltage when they commutate with high frequency.

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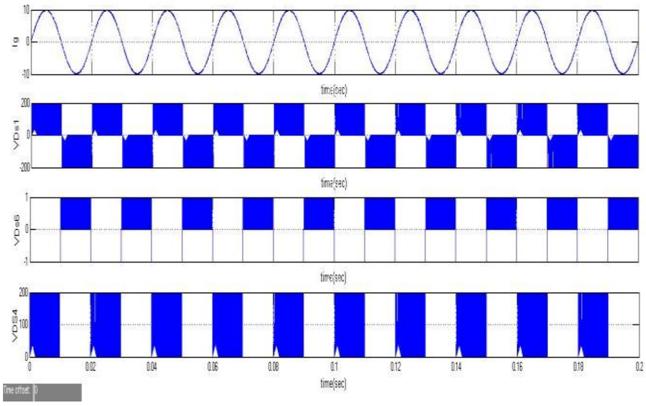

Figure 11: Grid current &switch voltages $V_{DS1}$, $V_{DS6}$ and $V_{DS4}$

The partial expansion of Figure 11 is provided that the switches S1 and S4 almost share the dc-link voltage when they commutate with high frequency. Therefore, the switching losses are minimized, and the results fulfill the theoretical analysis. The peak is same as grid peak current Im.

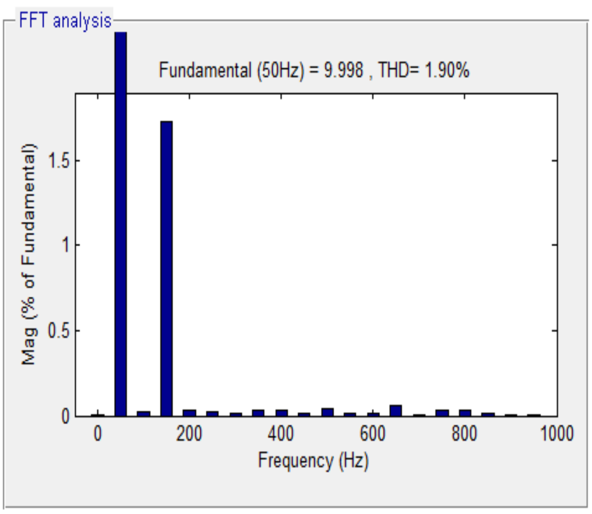


Figure 12: Total harmonic distortion of output current

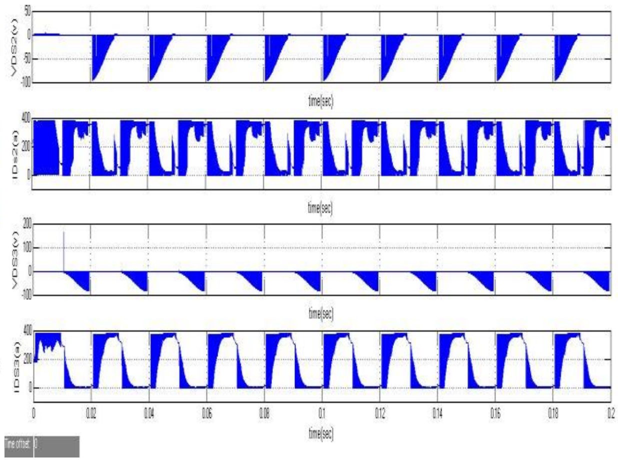

Figure 13: Voltages and currents of Switch S2 and S3

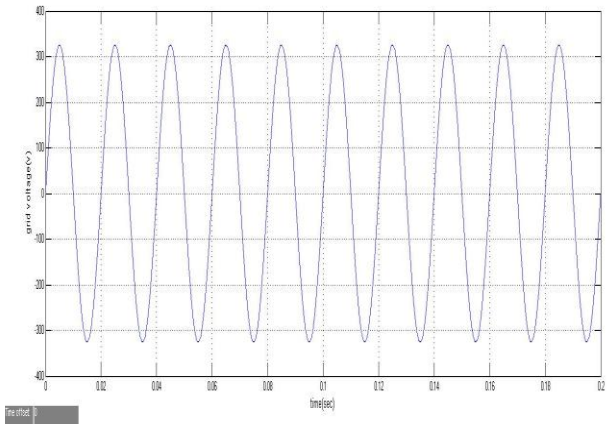

Figure 14: Grid voltage

## V CONCLUSION

In this paper, a family of new efficient transformerless inverter for grid-tied photovoltaic power generation system is presented using super-junction MOSFETs as main power switches. The main advantages of the proposed topology are as follows: (1) High efficiency over a wide load range is achieved by using MOSFETs and SiC diodes, (2) Like as isolated full-bridge inverter, excellent DM characteristics are achieved with unipolar SPWM, (3) PWM dead time is not required for main power switches, results low distortion at output

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