

# Efficient DTMF Detection based on Zynq 7000 Series of FPGA

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## ABSTRACT:

Dual-tone multi-frequency (DTMF) is a signaling standard in telecom applications that produces two tones simultaneously for each key press. By using efficient DTMF, this project divided into three phase's i.e. FFT, Split Goertzel Algorithm without Resource Sharing Approach, Split Goertzel Algorithm with Resource Sharing Approach. In these three phases we analyze area, timing & power. First phase is Fast Fourier Transform (FFT). In FFT, recursive operation is repeated N times. So that in FFT it requires more hardware, power & time. Second phase is split Goertzel Algorithm without Resource Sharing Approach. For high speed tone detection third technique i.e, Split Goertzel Algorithm with Resource Sharing Approach is used. Here, it uses predetermined frequencies & very minimal set of hardware, scheduled inputs & outputs are used at appropriate clock edges. So that it consumes less area & power. To detect DTMF detection a new type of ZYBO board ZYNQ 7000 series FPGA is used. Zynq is the combination of software & hardware systems. For functional verification Mentor Graphics Modelsim is used and for synthesis Xilinx ISE is used.

Keywords: DTMF, FFT, split Goertzel Algorithm without Resource Sharing Approach, split Goertzel Algorithm with Resource Sharing Approach., Xilinx ISE, FPGA, ZYNQ Platform.

## I.INTRODUCTION:

DTMF telephone keypad generates a sinusoidal tone and it is a mixture of two frequencies i.e., row and column frequencies. The below figure shows that, how the frequencies are organized:

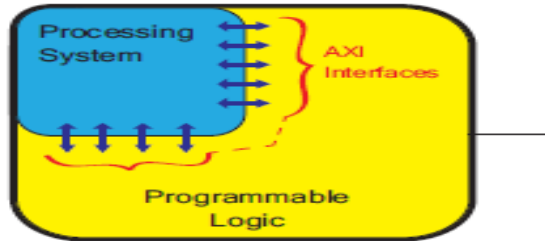
	Col 1 1209Hz	Col 2 1366Hz	Col 3 1477Hz	Col 4 1633Hz
Row 1 697 Hz	1	2	3	A
Row 2 770 Hz	4	5	6	B
Row 3 852 Hz	7	8	9	C
Row 4 941 Hz	*	0	#	D

Fig.1 Keypad represents high & low frequencies:

The DTMF keypad represents like a 4×4 matrix, with each column & each row represents as high & low frequencies. EX: If we press a single key (as '2') will gives a sinusoidal tone for each of the two frequencies (1336 hertz (Hz) and 697 Hz). DTMF is mainly used to develop for telecommunication equipment. DTMF is a standard where keystrokes from the telephone keypad are translated into dual tone signals over the audio link. FPGA'S are parallel processing devices and it is used to improve the performance of systems.

In this paper, Zynq platform plays vital role. It is the combination of both processing system and programmable logic. Here processing system is software, programmable logic is hardware. Zynq

is a platform; it combines a dual core ARM cortex\_A9 processor with traditional FPGA logic fabric. Zynq devices are more flexible. Processing system (PS) & Programmable logic (PL) are used independently or together, & separate power circuitry is configured for both PS and PL.



**Zynq Architecture**

**Fig.2**

Processing System is a hard processor. It exists as a dedicated and optimized silicon element on the device. Hard processors can achieve higher performance, for Zynq’s ARM processor. Programmable logic is a soft processor like the Xilinx Micro Blaze, which is formed by combining elements of the programmable logic fabric. The implementation of a soft processor is therefore the equivalent of any other IP block deployed in the logic fabric of an FPGA. In general, the advantage of soft processors is that the number and precise implementation of processor instances is flexible. One or more Micro Blaze soft processors can be used within the PL portion of the Zynq, to operate in conjunction with the ARM processor.

Processor works as the central element for hardware system. Software system runs through processor. Peripherals are functional components away from the processor

To achieve less area, low power, hardware optimized solution we use Spilt Goertzel Algorithm without RSA & Spilt Goertzel Algorithm with Resource Sharing Approach (RSA).

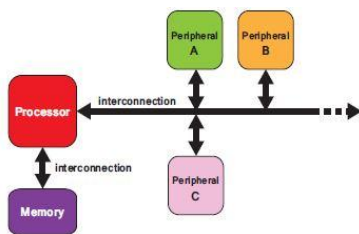
Mainly this paper divided into three phases.

Phase-I: In the first phase, by using Xilinx FFT core we can detect DTMF detection. The area, timing and power results are analyzed.

Phase-II: In the second phase spilt Goertzel Algorithm without Resource Sharing Approach is implemented. The area, timing and power results are analyzed.

Phase-III: In the third phase, spilt Goertzel Algorithm with Resource Sharing Approach is studied and suitable state machine based scheduling will be carried with limited resources to implement split Goertzel algorithm without RSA. The novel resource sharing based approach consumes less power and still it can detect efficient DTMF tones.

## II.IMPLEMENATION&DESIGN:



**Fig.3 Hardware Architecture of Zynq**

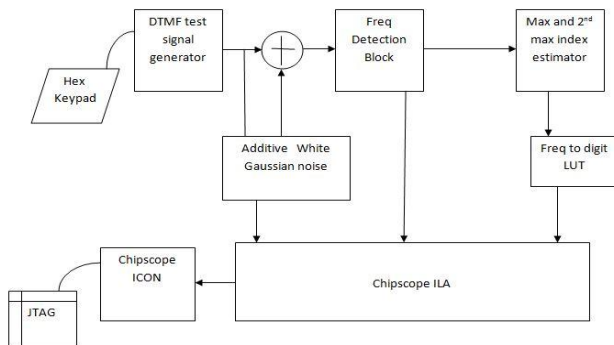


Fig.4 General Module DTMF Detection

The above figure represents General module DTMF Detection. It consists of six modules such as:

4x4 Hex key pad (input), Dual Tone Multi Frequency test signal generator, Additive white Gaussian noise, Frequency Detection block, Magnitude or index estimator and Frequency to digit look-up table.

Hex keypad is an external component and it act as input to DTMF module.

Frequency Test Signal Generator block generates necessary carrier frequencies. FTSG is again divided into two type's i.e, Frequency Word Selector & Direct Digital Synthesizer. FWS means, it selects frequency according to key pressed.

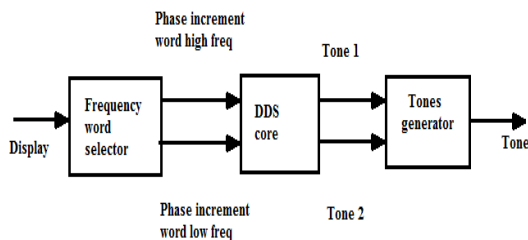


Fig. 5 Frequency Word Selector

DDS perform digital to analog conversation so that output will be in the form of analog usually a sine wave and this analog waveform combines with additive Gaussian noise then the output will be in the form of noise bits. This output gives as input to FDM i.e., Frequency Detection Module. Output will be in the form of magnitude indices. So that we can calculate 1<sup>st</sup> & 2<sup>nd</sup> max indices.

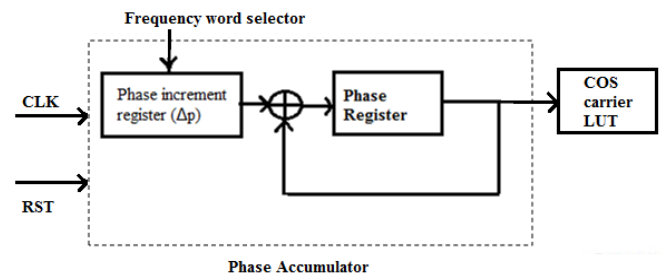


Fig. 6 Direct Digital Synthesizer

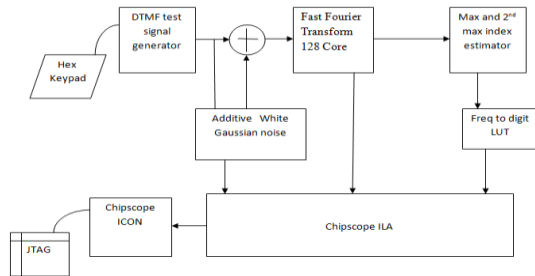
Chipscope ILA is used to monitor any internal signal of design. Chipscope ICON provides a communication path between Chipscope ILA & JTAG.

### III.EXISTING PROBLEM:

#### 1. FFT- 128 core:

FFT\_128 CORE is used instead of FDB. The Fast Fourier Transform (FFT) implements the Cooley-Tukey FFT algorithm, & FFT is an efficient algorithm to compute the discrete Fourier transform (DFT) and it's inverse. DFT decomposes a sequence of values into components of the different frequencies. DFT often too slow compare to FFT. FFT Algorithms mainly used in wide range of mathematics from complex number arithmetic to group theory and number theory. Input data presents in natural order and the output data can be in either natural or bit/digit reversed order. In FFT it consumes more power, area,

timing, & hardware. The below figure represents the FFT\_128 Core as Frequency Detection Module

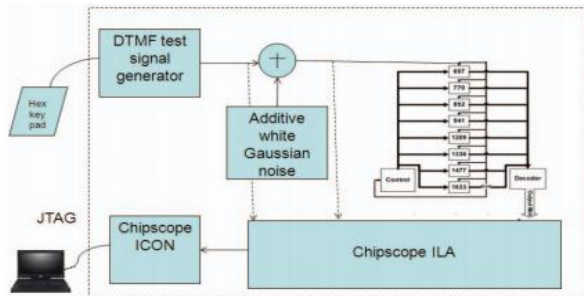


**Fig.7 Block Diagram with FFT-128 Core as Frequency Detection Module**

#### IV. PROPOSED SOLUTION:

##### 1. Spilt Goertzel Algorithm without Resource Sharing Approach.

The spilt Goertzel Algorithm without Resource Sharing Approach is a DSP technique; it is used to identify the frequency components of a signal, and published by Dr. Gerald Goertzel in 1958. Here spilt Goertzel Algorithm without Resource Sharing Approach module is added instead of FDB in DTMF Detection General Module.



**Fig.8 Spilt Goertzel Algorithm without Resource Sharing Approach as Frequency Detection Module**

Spilt Goertzel Algorithm without Resource Sharing Approach is used to reduce the no. of real value multiplications compare to DFT. In spilt Goertzel Algorithm without Resource Sharing Approach specific & predetermined frequencies will use. So that it consumes less area, low power. The Goertzel Algorithm performs tone detection using much less CPU horse power than the Fast Fourier Transform. Spilt Goertzel Algorithm without Resource Sharing Approach series for a length of N is:

$$H_k(Z) = \frac{1 - e^{j\frac{2\pi K}{N}} z^{-1}}{\left(1 - e^{j\frac{2\pi K}{N}} z^{-1}\right)\left(1 - e^{-j\frac{2\pi K}{N}} z^{-1}\right)}$$

$$K = 0, 1, \dots, N-1$$

##### 2. Spilt Goertzel Algorithm with Resource Sharing Approach.

Spilt Goertzel Algorithm with Resource Sharing Approach is an approach that, similar block of operations can assign. For example, +, to a common net list cell. Net list cells are be the resources; here net lists will be shared, so that it consumes less hardware. By using spilt Goertzel Algorithm without RSA we can implement spilt Goertzel Algorithm with RSA. In Goertzel algorithm all eight determined frequencies are appear, In spilt Goertzel Algorithm with RSA only 2 frequencies will used so that in spilt Goertzel Algorithm RSA consumes less hardware. The below figure shows spilt Goertzel Algorithm with Resource Sharing Approach.

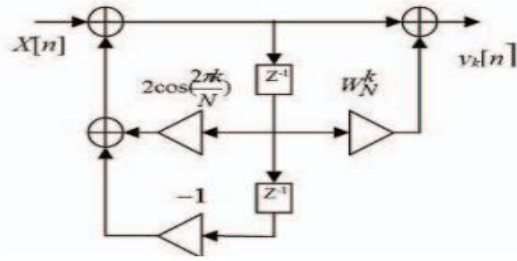


Fig.9 Split Goertzel Algorithm with Resource Sharing Approach

### V.SIMULATION AND SYNTHESIS RESULTS:

The below Figures represent the Simulation results for FFT, Split Goertzel Algorithm without Resource Sharing Approach, Split Goertzel Algorithm with Resource Sharing Approach.

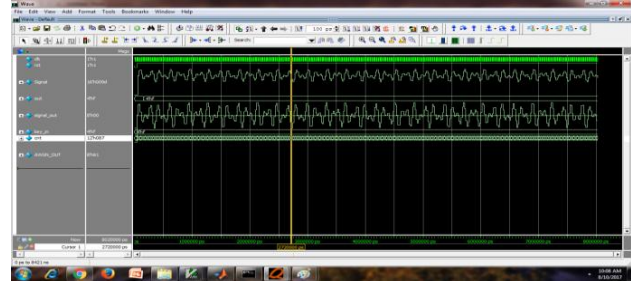


Fig. 11 Simulation Results of Split Goertzel Algorithm without Resource Sharing Approach

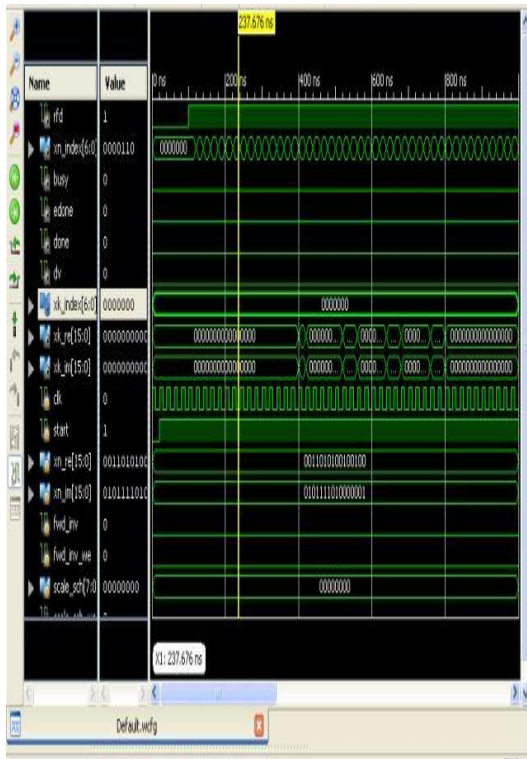


Fig.10 simulation Results of FFT

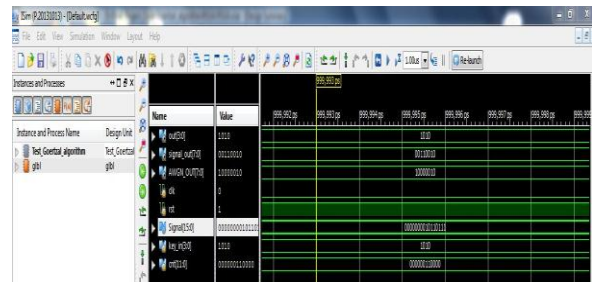


Fig.12 Simulation Results of Split Goertzel Algorithm with Resource Sharing Approach.

The Module, RTL Schematic, Device Utilization Summary are shown below by screenshots for FFT



Fig.13 Module of FFT

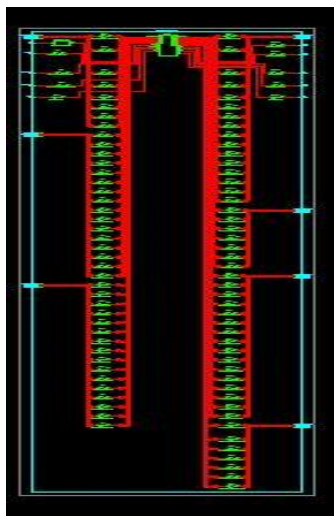


Fig.14 RTL Schematic of FFT

Table\_1: Device utilization Summary of FFT

Device Utilization Summary(estimated values)			
Logic Utilization	Used	Available	Utilization
Number Of Slice Registers	199	35200	5%
Number Of Slice LUTs	172	17600	9%
Number Of fully used	152	2191	69%

LUT-FF pairs			
Number Of bonded IOBS	96	100	96%
Number Of Block RAM/FIFO	4	60	6%
Number Of BUFG/BUFG CTRLS	1	32	3%
Number Of DSP 48E1S	9	80	11%

The below figures represent Module, RTL Schematic, Device Utilization Summary for Spilt Goertzel Algorithm without Resource Sharing Approach.

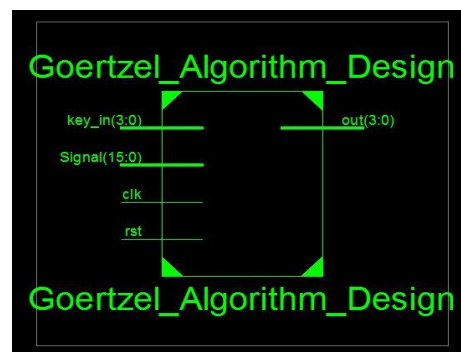


Fig. 15 Spilt Goertzel Algorithm without Resource Sharing Approach. Module



**Fig.16 RTL Schematic of Spilt Goertzel Algorithm without Resource Sharing Approach.**

**Table\_2: Device Utilization Summary of Spilt Goertzel Algorithm without Resource Sharing Approach.**

Device Utilization Summary(estimated values)			
Logic Utilization	Used	Available	Utilization
Number Of Slice Registers	1991	35200	5%
Number Of Slice LUTs	1727	17600	9%
Number Of fully used LUT-FF pairs	1527	2191	69%
Number Of bonded IOBS	96	100	96%
Number Of Block RAM/FIFO	4	60	6%
Number Of BUFG/BUFGCT RLS	1	32	3%
Number Of DSP 48E1S	9	80	11%

The below figures represent Module, RTL Schematic, Device Utilization Summary for Spilt Goertzel Algorithm with Resource Sharing Approach.



Fig. 17 RTL Schematic of Spilt Goertzel Algorithm with Resource Sharing Approach.

Table 3: Device Utilization Summary for Spilt Goertzel Algorithm with Resource Sharing Approach.

Logic Utilization	Used	Available	Utilization
Number Of Slice Registers	1	35200	0%
Number Of Slice LUTs	78	17600	0%
Number Of fully used LUT-FF pairs	12	79	15%
Number Of bonded IOBS	26	100	26%
Number Of BUFG/BUFGCTRLS	1	32	3%
Number Of DSP 48E1S	6	80	7%

Algorithm with RSA.

Table 5: Power results for Spilt Goertzel Algorithm with Resource Sharing Approach.

Device	On-chip	Power(w)	Used	Available	Utilization (%)
Family Zynq - 7000	Clocks	0	1	----	-----
Part Xc7z010	Logic	0	63	17600	0
Package Clg400	Signals	0	650	-----	-----
Temp Commercial	DSPS	0	21	80	26
Grade	IOS	0	26	230	11
process Typical	Leakage	0.01			
Speed -3	Total	0.01			
Grade					

ThermalProperties	Effective TJA(c/w)	Max Ambient(c)	Junction Temp(c)
	5.5	84.5	25.5

Supply Power(w)	Total	Dynamic	Quiescent
	0.100	0.00	0.100

Table 4: Power results for Spilt Goertzel Algorithm without Resource Sharing Approach.

Device	On-chip	Power(w)	Used	Available	Utilization (%)
Family Zynq - 7000	Clocks	0	1	----	-----
Part Xc7z010	Logic	0	61	17600	0
Package Clg400	Signals	0	259	-----	-----
Temp Commercial	DSPS	0	6	80	8
Grade	IOS	0	26	230	11
process Typical	Leakage	0.01			
Speed -3	Total	0.01			
Grade					

ThermalProperties	Effective TJA(c/w)	Max Ambient(c)	Junction Temp(c)
	5.5	84.5	25.5

Supply Power(w)	Total	Dynamic	Quiescent
	0.100	0.00	0.100

## V. CONCLUSION

In this project, we detect DTMF based FPGA implementation using Spilt Goertzel Algorithm with optimized Resource Sharing Approach. In the first phase, by using Xilinx FFT core we detected DTMF detection. The area, timing and power results are analyzed. The disadvantage of the DFT



technique is that it requires each harmonic to be calculated separately, which requires much more processing power, hardware & memory. In the second phase the split Goertzel algorithm without Resource Sharing Approach analysis is carried out. In the next phase the split Goertzel algorithm with Resource Sharing Approach is studied and suitable state Machine based scheduling will be carried with limited resources to implement split Goertzel algorithm without Resource Sharing Approach. To detect DTMF detection a new type of ZYBO board ZYNQ 7000 series FPGA is used. In FFT Total area consumed i.e; total gates used 2369, memory consumption 445818 kilo bytes & speed is 1.5ns. In FFT it consumes more area, power, speed. In Split Goertzel Algorithm without Resource Sharing Approach; Total area consumed i.e; total gates used 33, memory consumption 445818 kilo bytes & speed is 4.123ns. In Split Goertzel Algorithm with Resource Sharing Approach; Total area consumed i.e; total gates used 20, memory consumption 445818 kilo bytes & speed is 4.123ns. In Split Goertzel Algorithm with Resource sharing Approach can detect the incoming frequency within a  $\pm 1.5\%$  offset range. This algorithm does not check for overflow problems. So that it consumes less area, power & memory.

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