International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue 13
October 2017

Design for Testability of Sleep Convention Logic for memory applications

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ABSTRACT:
Non-volatile memory,NVM storage is a type of computer memory that can retrieve stored information even after having been power off.Flash memory is the type of this memory.here we are using flash memory.these memory is used for floating type transistors.The commodity memory is a high performancememory and embedded memories alone memories these are used for flash which has rapid growth when we go in the integrated chip. The flash memories have been Testedusing Conventional tests they are usually ad hoc.This is the procedure for testing which is expanded for certain designs.There is very much posibility of failure modes in this memories,automatic test equipment (ATE) is a test which is complicated and commonly seen. Production column and row address bit cell as basic design in SRAM. There will may be occurrence of sa0 and sa1 faults in anychip design, these faults will be overcome by using row,column address cells. we are making perfect location to store the data and making no cross sections of SRAMS. Extending of every cell checking for memory array and it gives verification of memory location. The row and column address buffer are used for picking the memory location. By comparing with previous method we used for the above two modules it gives accurate selection for memory location of cell check operation.

Keyword:

Design for Testability, Multithreshold Null Convention Logic, Null Convention Logic, Sleep Convention Logic.

1. INTRODUCTION

The important role play of SRAM is increased in applications of soc. The Statius is giving the total area of chip exceeded 50% by SRAM. As Reported by development of 6T-SRAM cells using the standard CMOS processes as (3.87um2 for 0.18um1 and 1.87um2 for 0.13um technology node) and these cells are most suited for using inSOC(system on chip) to the requirement of high-density and performanceand also vastly manufactured.

For making sure that their reliability and robustness and manufacturability,are the normal PCM structures of test are not adequate to monitor high density SRAM process, so that because of specific interactions in between SRAM process and design.normally PCMs are havingmuch generic nature and are kept for supportfor process module of robust development.so that,the structures here are not regularly allow us for testing the power of choosen design of SRAM rule of environment for specifically Static RAM.This structure is not much suited for providing response of SRAM chips.The layer features of SRAM are very much complex.

DFT is important in this system on chip design and semiconductor industry so that it is essential to reduce testtime, increase the quality of test. and decrease the amount associatedwith applying and the tests are generated here to theNCL(null convention logic) circuit.No Designfor testability method is developing for theSCL(sleep convention logic) circuits. The current NCL specific DFT techniquescan not be once used for this circuitbecause of thestructural changes made by introduction of the sleepmechanism known as power-gating technique. The main purpose of the project is for analyzing the types of faults sa0 and sa1present in the sleep convention logicpipeline andto introduce a full scan testmethod whichprovides a fully testinganalises at very less ammount that is at cost of the areaoverheard that is get by proposing the scan technique.

II.DESCRIPTION OF THE TESTING STRUCTURES

The parameters of electrical things are using to prove the good conditions of our Static RAM designs it also Measures the current which is leaked and the arrangement of inter and intra-layer,the measuring of resistance is used for integrity testing connections,theSRAM features to the monitor, and makingnecessarychanges from targets, beta ratio, the evaluation of static noise margin for designing of Static RAM's functional robustness.

The design for testing should be sensitive so that it should check the process of therandom and systamatic occurrences of any weakness of cell memory.this may also used to changing the transistors of SRAM for accuracies,beta ratios and static noise under the SRAM area. Hence, in this test chip of qualification of SRAM, SRAM is testing the structures of SRAM have been designed by us so that for ensuring the SRAM cell in good condition and the SRAM features.

For making sure the manufacturability of this Static RAM cells,here the series of test cells are designed,they are aimed Static RAM cells. Every part is being tested. Every cell changesshows us for testing good conditions and robustness requiring in the SRAM cell.Using the improved Static RAM cells for building the big arrays the SRAM cells are repeated. The parameters like (resistance,current leaking) is the complete array and it would be measured.so that full information is formed from a hugecells of SRAM chip,so that the confidence level will be increased of quality of robustness of every feature. The particular structures of array around very much helpfull for checking the design modifications of SRAM cells so that they further improving the design,shows us the come back on critical design rules of changes and ultimatelyused for quick testing of proposed process of Static RAM design.

Despite of these applications, adoptation ofsleep convention logic in industryis on many factors, keeping the developmentofnew promising NCLlogic style. The purpose of research is to propose comprehensiveDFT method for Sleep Conventional Logic.The DFT method is basing on scan design, this isvery famous in industry,this is providing for full testing.The testingis done for every certain cell in SCL,the efficiencyis proved.Atlast the following contributionsare done.

1) The sa0 and sa1 in certainSCL pipeline is analized here.

2) A scan-based design for testability method isproposed and by considering the faults.

3) This method is compatible with thecurrent state and ATPG tools.

4) This design for testability is given to a numberof Sleep Convention Logic circuits, and the result is shown in high test coverageat the low cost.

III. PROPOSED METHOD

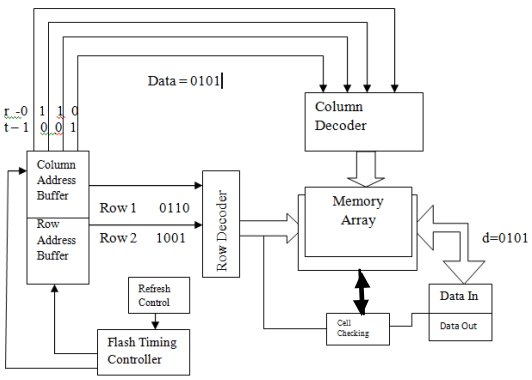

Fig 1 Proposed system

There is no cell checking operation in the existingsystem so that it may not verify the memory location twice.In this system There is single memory cell array so that to send the data in single phase. There are the two problems in existing system, to overcome these two problems we are proposing a new architecture in this system.

The proposed system is consisting of refresh control, cell checking, memory array, flash timing controller, column address buffer, row address buffer, column decoder, row decoder, data in or data out.

The refresh controller and the flash controller will refresh all the data in the memory array location is refreshed. The column address buffer and row address buffer will send the buffer of address and it may be column or row. The address buffer is taken itself by their respective decoder, which means column address buffer is given to the column decoder and the buffer address is decoded.

The output of row and column decoder.This will select the memory location in the memory array. As the changing of row or column address buffer the decoder will be changing the memory location. The total memory location will call it as the memory array.

The cell checking blocks will check either to select the memory location array i.e. S=0 or 1. If S=0 then the memory location array one will be selected, and data is impend in the array memory location. Else S=1 the second array memory location will be selected and then the data impend in second memor location.

The date-in used for writing the data and data-out is used for reading the data memory array. By using this proposed system we are overcoming the checking of the memory array and the array of two memory locations.

IV.RESULTS AND DISCUSSIONS

The total output is shown in figure per the address of row and column the data is stored in that respective memory location showm below.

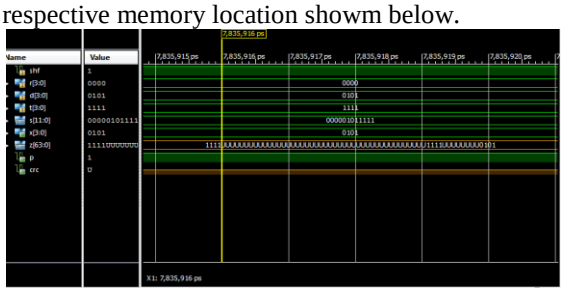

Fig 2 Technology Schematic

We are testing the faults in the chip by giving three inputs namely u,v,x and output is given as c.if the output is same as input then there is no faults in this chip and if the output is changed then there may occur the fault and the chip doesnot work properly.so as shown in the above result there are no faults as the output is same input so there is no faults present in my result.

V.CONCLUSION

As that here are number of failure modes for memories of flash. algorithms of testing that is (ATE)which is complicated are normally seen here. Production row address bit cell and column address bit cell for any weaknesses of method. There may be occurrence of sa0 and sa1 faults(stuck at faults) in any chip design, these faults are overcome by using row address cell and column address cells we make perfect location for storing the data and there is no cross sections of SRAMS. By extending the cell checking for memory array gives the verification of memory location. The column address buffer and the row address buffer are used to pick the memory location. By comparing with the previous method the above two modules gives the accurate selection of the memory location of the cell checking operation.

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