International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue 13
October 2017

High Speed Fault Tolerant Parallel Ffts Using Error Correction And Detection Codes

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ABSTRACT: The complexity of communications and signal processing circuits increases every year. This is made possible by the CMOS technology scaling that enables the integration of more and more transistors on a single device. This increased complexity makes the circuits more vulnerable to errors. At the same time, the scaling means that transistors operate with lower voltages and are more susceptible to errors caused by noise and manufacturing variations. Soft errors pose a reliability threat to modern electronic circuits. This makes protection against soft errors a requirement for many applications. Communications and signal processing systems are no exceptions to this trend. For some applications, an interesting option is to use algorithmic-based fault tolerance (ABFT) techniques that try to exploit the algorithmic properties to detect and correct errors. Then, two improved protection schemes that combine the use of error correction codes and Parseval checks are proposed and evaluated. The results show that the proposed schemes can further reduce the implementation cost of protection. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.

***Index Terms*—Error correction codes (ECCs), fast Fourier transforms (FFTs), soft errors.**

I.INTRODUCTION

Electronic circuits are increasingly present in automotive, medical, and space applications where reliability is critical.

need is further increased by the intrinsic reliability challenges of advanced CMOS technologies that include, e.g., manufacturing variations and soft errors. A number of techniques can be used to protect a circuit from errors. Those range from modifications in the manufacturing process of the circuits to reduce the number of errors to adding redundancy at the logic or system level to ensure that errors do not affect the system functionality. To add redundancy, a general technique known as triple modular redundancy (TMR) can be used.

The TMR, which triplicates the design and adds voting logic to correct errors, is commonly used. However, it more than triples the area and power of the circuit, something that may not be acceptable in some applications. When the circuit to be protected has algorithmic or structural properties, a better option can be to exploit those properties to implement fault tolerance. One example is signal processing circuits for which specific techniques have been proposed over the years. Digital filters are one of the most commonly used signal processing circuits and several techniques have been proposed to protect them from errors.

Most of them have focused on finite-impulse response (FIR) filters. For example, the use of reduced precision replicas was proposed to reduce the cost of implementing modular redundancy in FIR filters. In a relationship between the memory elements of an FIR filter and the input sequence was used to detect errors. Other schemes have exploited the FIR properties at a word level to also achieve fault tolerance. The use of residue number systems and arithmetic codes has also been proposed to protect filters.

Finally, the use of different implementation structures of the FIR filters to correct errors with only one redundant module has also been proposed. In all the techniques mentioned so far, the protection of a single filter is considered. However, it is increasingly common to find systems in which several filters operate in parallel. This is the case in filter banks and in many modern communication systems. For those systems, the protection of the filters can be addressed at a higher level by considering the parallel filters as the block to be protected. This idea was explored, where two parallel filters with the same response that processed different input signals were considered. It was shown that with only one redundant copy, single error correction can be implemented. Therefore, a significant cost reduction compared with TMR was obtained.

In this brief, a general scheme to protect parallel filters is presented. As parallel filters with the same response that process different input signals are considered. The new approach is based on the application of error correction codes (ECCs) using each of the filter outputs as the equivalent of a bit in and ECC codeword. This is a generalization of the scheme presented and enables more efficient implementations when the number of parallel filters is large. The scheme can also be used to provide more powerful protection using advanced ECCs that can correct failures in multiples modules.

II. ERROR TOLERANT TECHNIQUES FOR PARALLEL FFTS

A. Error Correction based on Hamming Codes

The aim of error tolerant design is to protect parallel FFTs from errors. Various schemes have been proposed for error detection and correction in FFTs. One of the basic and simple methods is error correction using hamming codes. Unlike parity code which can detect only odd bit error, the hamming code can detect two bit errors and correct one error.

Similar to other error correction codes, hamming codes also utilizes the parity bit which is generated for the corresponding input sequence for detecting errors. It achieves higher code rate with minimum distance of three. The number of parity bits depends on the total number of data bits.

B. Fault tolerant FFT based on Parseval's Check

Parseval's method is one of the techniques to detect errors parallel in multiple FFT. This is achieved with Sum of Squares (SOSs) check based on Parseval's theorem. The error free FFT should have its Sum of Squares of the input equaling the Sum of Squares of its frequency domain output.

This correlation can be used to identify errors with minimum overhead. For parallel

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FFTs, the Parseval's check can be combined with the error correction codes to minimize the area overhead. Multiple error detection and correction is achieved through this combination. One of the easy ways is to generate the redundant input for single FFT with all the four FFT inputs. To correct error the parity FFT output is XORed with fault free outputs of the FFTs.

Compared to the previous schemes presented in the Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks, this technique reduced the total number of Sum of Squares used. Another existing work done is by combining SOS checks with hamming codes instead of using Parseval's check individually as shown in Fig. 1

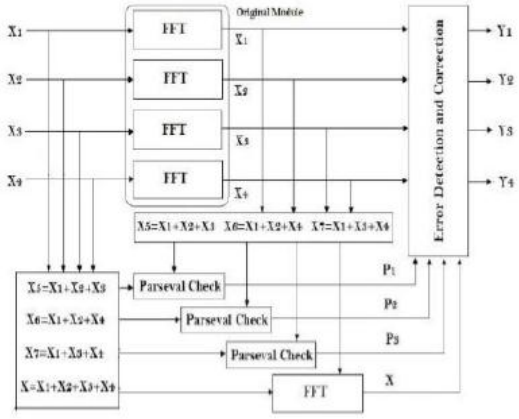

Fig 1. Parity-SOS-ECC fault-tolerant parallel FFTs

Sum of Squares is thus eliminated using only the adder blocks. Technique 1 also uses 3 parallel redundant.

This method combines the feature of parity calculation of hamming codes and error detection process of Sum of Squares. Concurrent Error Detection (CED) schemes for the FFT are the Sum of Squares (SOS) check based on Pa theorem. The use of parseval check is exponentially reduced to the direct comparisons of FFTs inputs and outputs used to protect parallel FFTs.

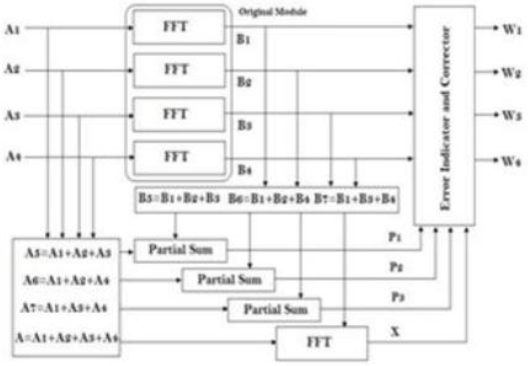

Fig 2. The new technique which focuses on the existing systems

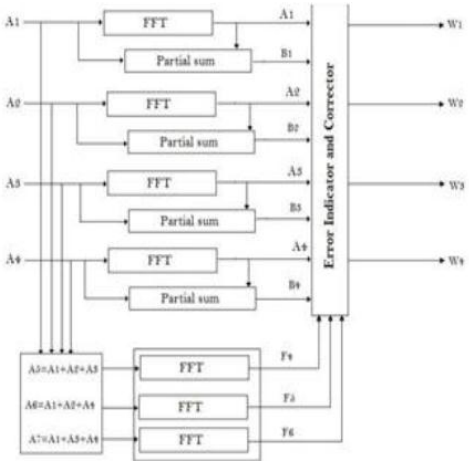

Fig 3. Parity-PS-ECC fault-tolerant parallel FFTs

III. PROPOSED ERROR INDICATOR AND CORRECTOR TECHNIQUES

The proposed work focuses on two new techniques for reducing the hardware overhead and increasing the error correction capability. The Fig.2 describes the new technique which focuses on the existing systems limitations.

The technique analyzed in the previous work has certain limitation due to the complexity of handling larger number of FFTs and Sum of Squares block. Instead of using Sum of Squares, Partial summation is used for calculating its parity at the input and the output side of the FFT. It sums all possible node values of 4-point FFT along with the twiddle factors. Multiplication operation which leads to the complexity in Fig.3 illustrates the Parity Partial Summation block for less error prone applications. For example when the error occurs in A1 and A2 then it can be detected by the partial summation used individually for FFT blocks. The first check equation is selected in such a way that the both error block signals are not present.

In all the techniques discussed, soft errors can also affect the elements added for protection. For the ECC technique, the protection of these elements was discussed. In the case of the redundant or parity FFTs, an error will have no effect as it will not propagate to the data outputs and will not trigger a correction. In the case of SOS checks, an error will trigger a correction when actually there is no error on the FFT. This will cause an unnecessary correction but will also produce the correct result. Finally, errors on the detection and correction blocks can propagate errors to the outputs.

In our implementations, those blocks are protected with TMR. The same applies for the adders used to compute the inputs to the redundant FFTs or to the SOS checks. The triplication of these blocks has a small impact on circuit complexity as they are much simpler than the FFT computations. A final observation is that the ECC scheme can detect all errors that exceed a given threshold (given by the quantization used to implement the FFTs). On the other hand, the SOS check detects most errors but does not guarantee the detection of all errors. Therefore, to compare the three techniques for a given implementation, fault injection experiments should be done to determine the percentage of errors that are actually corrected. This means that an evaluation has to be done both in terms of overhead and error coverage.

IV.RESULTS

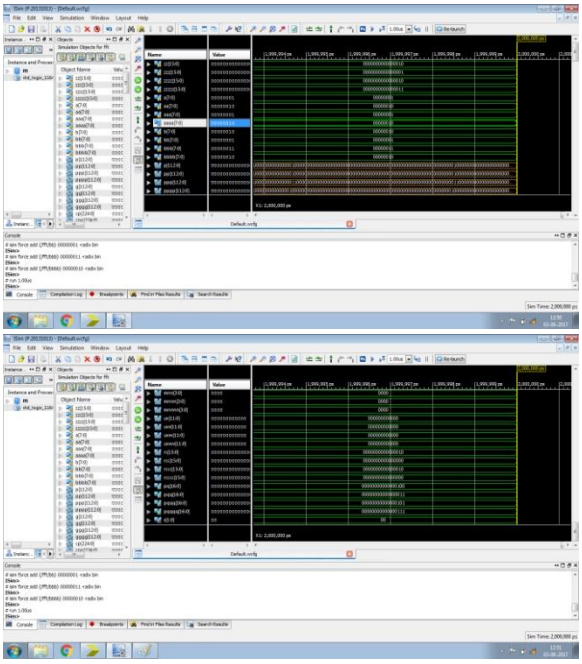

Fig 3. Output waveform

V.CONCLUSION

Detecting and correcting errors such as critical reliability are difficult in signal processing which increases the use of fault tolerant implementation. In modern signal processing circuits, it is common to find several filters operating in parallel. Proposed is an area efficient technique to detect and

correct single errors. This brief has presented a new scheme to protect parallel FFT using cordic that is commonly found in modern signal processing circuits.

The approach is based on applying SOS-ECC check to the parallel FFT outputs to detect and correct errors. The SOS checks are used to detect and locate the errors and a simple parity FFT is used for correction. The 8 point FFT with the input bit length 32 is protected using the proposed technique. . The detection and location of the errors can be done using an SOS check per FFT or alternatively using a set of SOS checks that form an ECC. This technique can detect and correct only single bit error and it reduces area results in high speed compared to existing techniques.

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