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High Speed Redundant Binary Multipliers Using Ppp and Ppg

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ABSTRACT: Adders are the key element of the arithmetic unit, especially fast parallel adder. Redundant Binary Signed Digit (RBSD) adders are designed to perform high-speed arithmetic operations. Generally, in a high radix modified Booth encoding algorithm the partial products are reduced in multiplication process. Due to its high modularity and carry-free addition, a redundant binary (RB) representation can be used when designing high performance multipliers. The conventional RB multiplier re-quires an additional RB partial product (RBPP) row, because an error-correcting word (ECW) is generated by both the radix-4 Modified Booth encoding (MBE) and the RB encoding. This incurs in an additional RBPP accumulation stage for the MBE multiplier.

In this paper, a new RB modified partial product generator (RBMPPG) is proposed; it removes the extra ECW and hence, it saves one RBPP accumulation stage. Therefore, the proposed RBMPPG generates fewer partial product rows than a conventional RB MBE multiplier. Simulation results show that the proposed RBMPPG based designs significantly improve the area and power consumption when the word length of each operand in the multiplier is at least 32 bits.

Index Terms—Redundant binary, modified booth encoding, RB partial product generator, RB multiplier

I.INTRODUCTION

Digital multipliers are widely used in arithmetic units of microprocessors, multimedia and digital signal processors. Many algorithms and architectures have been proposed to design high-speed and low power multipliers. A normal binary (NB) multiplication by digital circuits includes three steps.

In the first step, partial products are generated; in the second step, all partial products are added by a partial product reduction tree until two partial product rows remain. In the third step, the two partial product rows are added by a fast carry propagation adder. Two methods have been used to perform the second step for the partial product reduction. A first method uses 4-2 compressors, while a second method uses redundant binary (RB) numbers. Both methods allow the partial product reduction tree to be reduced at a rate of 2:1.

The redundant binary number representation has been introduced by Avizienis to perform signed-digit arithmetic; the RB number has the capability to be represented in different ways. Fast multipliers can be designed using redundant binary addition trees.

Alternatively, a high-radixBooth encoding technique can reduce the number of partial products. However, the number of expensive hard multiples (i.e., a multiple that is not a power of two and the operation cannot be

performed by simple shifting and/or complementation) increases too. Besliet al. noticed that some hard multiples can be obtained by the differences of two simple power-of-two multiplies. A new radix-16 Booth encoding (RBBE-4) technique without ECW has been proposed; it avoids the issue of hard multiples. A radix-16 RB Booth encoder can be used to overcome the hard multiple problem and avoid the extra ECW, but at the cost of doubling the number of RBPP rows. Therefore, the number of radix-16 RBPP rows is the same as in the radix-4 MBE.

However, the RBPP generator based on a radix-16 Booth encoding has a complex circuit structure and a lower speed compared with the MBE partial product generator [10] when requiring the same number of partial products. The aim of this study is implementation of modified partial product generator for RB multipliers.

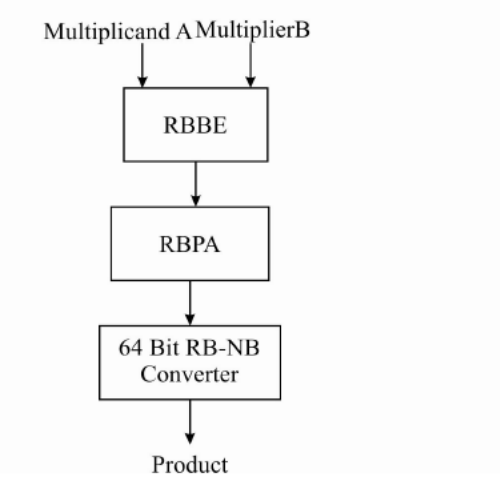

Fig.1. BLOCK DIAGRAM

A RB multiplier consists of a RB partial product (RBPP) generator, a RBPP reduction tree and a RB-NB converter. A Radix-4 Booth encoding or a modified Booth encoding (MBE) is usually used in the partial product generator of parallel multipliers to reduce the number of partial product rows by half. A RBPP row can be obtained from two adjacent NB partial product rows by inverting one of the pair rows.

II. RADIX -4 BOOTH ENCODING

Booth encoding has been proposed to facilitate the multiplication of two's complement binary numbers. It was revised as modified Booth encoding (MBE) or radix-4 Booth encoding. The multiplier bits are grouped in set of three adjacent bits. The two side bits are overlapped with neighboring groups except the first multiplier bits group in which it is {b1, b0, 0}. Each group is decoded by selecting the partial product, where 2Aindicates twice the multiplicand, which can be obtained by left shifting. Negation operation is achieved by inverting each bit of A and adding '1' (defined as correction bit) to the LSB.

III. RB PARTIAL PRODUCT GENERATOR:

As two bits are used to represent one RB digit, then a RBPP is generated from two NB partial products. The addition of two N-bit NB partial products X and Y using two's complement representation can be expressed as follows

$$X + Y = X - Y - 1$$
$$= (X, Y) - 1$$

The RBPP is generated by inverting one of the two NB partial products and adding -1 to the LSB. Each RB digit X_i belongs to the set {-1,0,1}; this is coded by two bits (X_i^-, X_i^+) .RB numbers can be coded in several ways.

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Both MBE and RB coding schemes introduce errors and two correction terms are required: 1) when the NB number is converted to a RB format, -1 must be added to the LSB of the RB number; 2) when the multiplicand is multiplied by -1 or -2 during the Booth encoding, the number is inverted and +1 must be added to the LSB of the partial product. A single ECW can compensate errors from both the RB encoding and the radix-4 Booth recoding.

IV.PROPOSED RB PARTIAL PRODUCT GENERATOR

A new RB modified partial product generator based on MBE (RBMPPG-2) is presented in this section; in this design, ECW is eliminated by incorporating it into both the two MSBs of the first partial product row (PP_1^+) and the two LSBs of the last partial product row ($PP^-_{(N/4)}$).

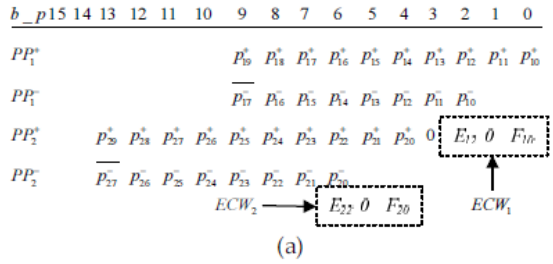

Fig 2(a). THE FIRST NEW RBMPPG-2 ARCHITECTURE FOR AN 8-BIT MB MULTIPLIER

It is differ from conventional type by its error correcting vector. In this type error correcting vectors ECW1 is generated by PP1 and ECW2 is generated by PP2.

ECW1= 0 E_{12} 0 F_{10}

ECW2= 0 E_{22} 0 F_{20}

To eliminate a RBPP accumulation, ECW 2 needs to be incorporated into PP1 and PP2.

F 20= {-1, b5 b4 b3=000,001,010,011,111

F20= {0, b 5b4b3=100,101,110

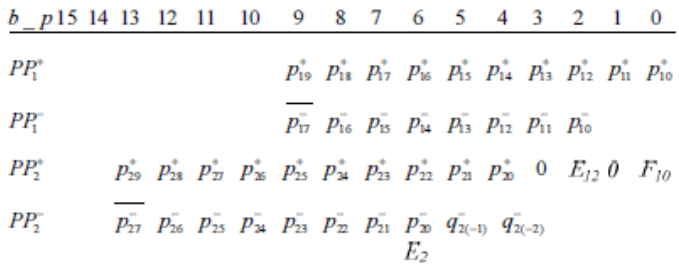

Fig 2(b) REVISED RBMPPG BY REPLACING E $_{22}$ AND F $_{20}$

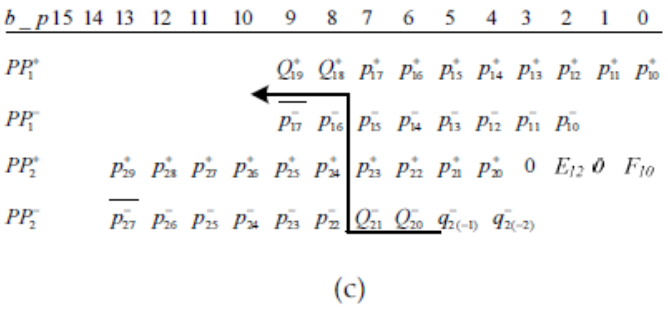

Fig2(c) FINAL PROPOSED RBMPPG BY TOTALLY ELIMINATING ECW $_2$

Q_{19}^+ ,Q_{18}^+,Q_{21}^-,Q_{20}^- are used to represent the modified partial products .By setting $PP2^+$ to all ones and adding +1 to the LSB of the partial product ,F_{20} can then be determined only by b_5

F_{20} = {-1, b_5 =0

F_{20}= {0, b_5 =1

As -1 can be coded as 111 in RB format, E_{22} and F_{20} can be represented by E_2 ,$q_{2(-2)}^-$,$q_{2(-1)}^-$ as follows

$$E_2 = \begin{cases} E_{22}, & F_{20} = 0 \\ E_{22} - 1, & F_{20} = -1 \end{cases}$$

$$q^-_{2(-2)} = q^-_{2(-1)} = \begin{cases} 0, & F_{20} = 0 \\ 1, & F_{20} = -1 \end{cases}$$

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Logic functions of Q_{19}^{+} ,Q_{18}^{+},Q_{21}^{-},Q_{20}^{-} can be expressed as follows

$$Q_{19}^{+} = (b_7 \oplus b_5 + b_7 b_6 b_5) \cdot p_{19}^{+} + \overline{b_7}\,\overline{b_5} \cdot (p_{18}^{+} + p_{21}^{-} + p_{19}^{+}) + b_7 \overline{b_6} b_5 \cdot (p_{18}^{+} p_{21}^{-} p_{20}^{-} \oplus p_{19}^{+})$$

$$Q_{18}^{+} = (b_7 \oplus b_5 + b_7 b_6 b_5) \cdot p_{18}^{+} + \overline{b_7}\,\overline{b_5} \cdot (\overline{p_{21}^{-} + p_{20}^{-}} \oplus p + b_7 \overline{b_6} b_5 \cdot (p_{21}^{-} p_{20}^{-} \oplus p_{18}^{+})$$

$$Q_{21}^{-} = (b_7 \oplus b_5 + b_7 b_6 b_5) \cdot p_{21}^{-} + \overline{b_7}\,\overline{b_5} \cdot \overline{p_{21}^{-} \oplus p_{20}^{-}} + b_7 \overline{b_6} b_5 \cdot p_{21}^{-} \oplus p_{20}^{-}$$

$$Q_{20}^{-} = (b_7 \oplus b_5 + b_7 b_6 b_5) \cdot p_{20}^{-} + \overline{b_7}\,\overline{b_5} \cdot \overline{p_{20}^{-}} + b_7 \overline{b_6} b_5 \cdot \overline{p_{20}^{-}}$$

TABLE III

Therefore, the extra ECWN/4 is removed by the transformation of 4 partial product variables and one partial product row is saved in RB multipliers with any power-of-two word-length.

In the second stage, a 4-stage RBA summing tree is used to sum 16 RB partial products. Each RBA block contains 64 RB full adder (RBFA) cells and a varying number of RB half adder (RBHA) cells depending on where it is located**.** The proposed RBMPPG-2 can be applied to any bit RB multipliers with a reduction of a RBPP accumulation stage compared with conventional designs. Although the delay of RMPPG-2 increases by 1-stage of TG delay, the delay of one RBPP accumulation stage is significantly larger than a 1-stage TG delay. Therefore, the delay of the entire multiplier is reduced. The improved complexity, delay and power consumption are very attractive for the proposed design. The multiplier consists of the proposed RBMPPG-2, three RBPP accumulation stages, and one RB-NB converter. Eight RBBE-2 blocks generate the RBPP they are summed up by the RBPP reduction tree that has three RBPP accumulation stages. Each RBPP accumulation block contains RB full adders (RBFAs) and half adders (RBHAs).

The 64-bitRB-NB converter converts the final accumulation results into the NB representation, which uses a hybrid parallel prefix/carry select adder.

VI.RESULTS

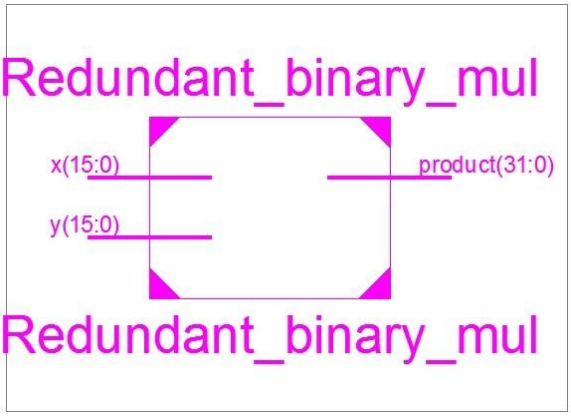

Fig 3. RTL SCHEMATIC

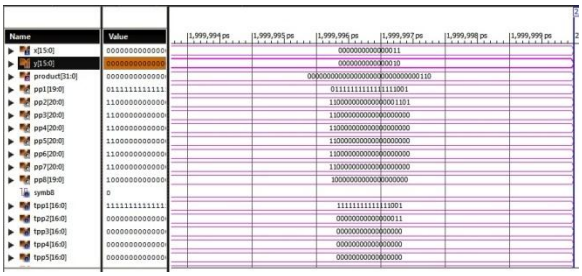

Fig 4. OUTPUT WAVEFORM

VII.CONCLUSION

A new modified RBPP generator has been proposed in this paper; this design eliminates the additional ECW that is introduced by previous designs. Therefore, a RBPP accumulation stage is saved due to the elimination of ECW. The new RB partial product generation technique can be applied to any 2n-bit RB multipliers to reduce the number of RBPP rows from N/4 + 1 to N/4. Simulation results have shown that the performance of RB MBE multipliers using

the proposed RBMPPG-2 is improved significantly in terms of delay and area. The proposed designs achieve significant reductions in area and power consumption when the word length is at least 32 bits.

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