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A High Speed hybrid FIR Filter Architecture for Fixed and Reconfigurable Applications

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ABSTRACT: *The main intent of FIR filters is to settle the impulse response zero in finite time. The filter may be discrete time or continuous time and analog or digital. In this paper for the purpose of better performance we use transpose form finite impulse response (FIR) filters. This filters are inbuilt pipe lined and it supports multiple constant multiplication (MCM) technique for saving estimation of filters. Based on the estimation analysis of transpose form of FIR filter the flow graph will be optimized for better complexity. Here transpose form does not directly support the block processing but there is a possibility of realization. In the proposed structure, there are two implementations one is less area delay product (ADP) and less energy per sample (EPS). Direct form FIR structure has less ADP and EPS than the proposed structure. So from the result of application specific integrated circuit synthesis, it shows that the proposed structure has block size 4 and filter length 64. This involves 42% less ADP and 40% less EPS than available FIR filter. Now let us see the result for the same block size and proposed structure involves 13% less ADP and 12.8% less EPS compared to proposed direct form block FIR structure.*

I.INTRODUCTION

Generally, finite impulse response is analog or digital filters but in this we are assuming that FIR is a digital filter. This is mostly used in various applications like speech processing, loud speaker equalization, echo cancellation and so on. Large FIR filters are needed to get frequency specifications for these filters. For very high speed digital communication we use FIR filters which consists of high sampling rate. Foe every filtered output the number of multiplications and additions are required, this increases the order of filters linearly.

The coefficients in filter are constant are known as prior in signal processing applications. To reduce the complexity of realization of multiplications. To derive high throughput hardware structures, block processing method is used. This method increases the efficiency of area delay .In transpose form configuration this method does not support directly but it offers high operating frequency. Many designs have been proposed from last few decades but for better realization we use reconfigurable FIR (RFIR) filters with general multiplier and constant multiplication. In RFIR filter architecture computation sharing vector scaling technique is proposed. In this technique cannon sign digit (CSD) based RFIR filter is used. Here the non zero CSD values are obtained which reduces the precision of filter coefficients. But the recognition process doesn't provide an area delay. Efficient structure SDR channel is one of application of FIR filter. The constant shift method and programmable shift method are the proposed RFIR filters, this methods are used in SDR channel. Actually there are two configurations 1) transpose from configure and 2) direct form configuration. Multiplier less structures are used in transport from configuration and DA-based structures are used in direct from configuration, these proposed design method are suitable for 2-D FIR filter.

II. COMPUTATIONAL ANALYSIS AND MATHEMATICAL FORMULATION OF BLOCK TRANSPOSE FORM FIR FILTERS

FIR filter output of length N can be related as

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$$y(n) = \sum_{i=0}^{N-1} h(i) \cdot x(n-i).$$

The above equation can be expressed by a recurrence relation as

$$Y(z) = [z^{-1}(\cdots(z^{-1}(z^{-1}h(N-1) + h(N-2)) + h(N-3)) \cdots + h(1)) + h(0)]X(z). \quad (2)$$

A. Computational Analysis

In this we use two data flow graphs , it is represented as DFG-1 &DFG-2 and these two data flow graph are in transpose Form of FIR filter length N=6 . This Is shown in fig(1) . It has two blocks and their inputs are represented as x (n) & x(n-1) In the similar way output is represented as y(n) & y(n-1) . Fig (2) shows the product values and their acclamation paths of data flow graphs 1&2. The arrow that represents in fig(2) are the accumulation paths of products.

In fig (2) redundant applications are obtained in both data flow graphs. This can be avoided by using non overlapping sequence which is shown in figure(3). fig3(a) represents DFT-3 for computation of y (n) and fig3(b) represents DFT-4 for computation of y (n-1).

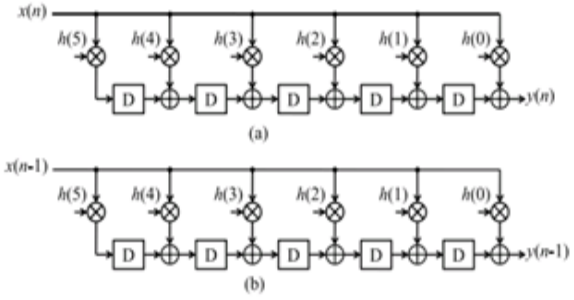

Fig. 1. DFG of transpose form structure for N = 6. (a) DFG-1 for output y(n). (b) DFG-2 for output y(n − 1)1703

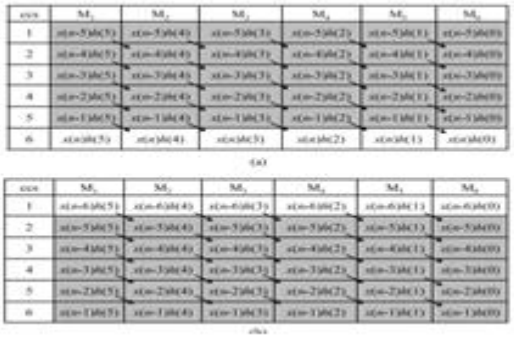

Fig. 2. (a) DFT of multipliers of DFG shown in Fig. 1(a) corresponding to output y(n). (b) DFT of multipliers of DFG shown in Fig. 1(b) corresponding to output y(n − 1). Arrow: accumulation path of the products.1703

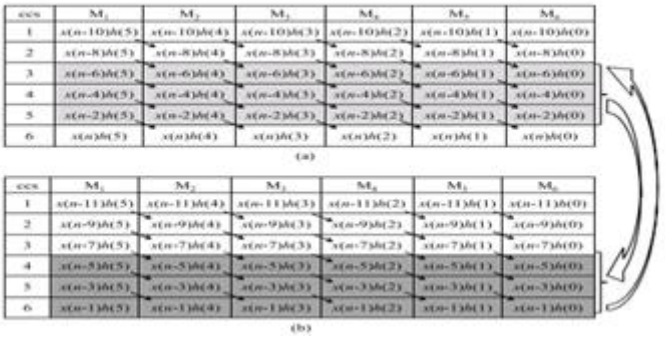

Fig. 3. DFT of DFG-1 and DFG-2 for three non overlapped input blocks [x(n), x(n −1)], [x(n −2), x(n −3)], and [x(n −4), x(n −5)]. (a) DFT-3 for computation of output y(n). (b) DFT-4 for computation of output y(n − 1).1703

B. DFG transformation

The both DFT's 3&4 are realized from data flow graph-3 which consists of non overlapping blocks as shown in figure(4) . In this transpose from type-1 configuration of block FIR filters are used. Fig (5) represents the block transpose from type-2 configuration. In this block transpose from type -3 is obtained. The both type-1& type-2 configuration has same number of multiplier and address. Type -2 configuration derives the proposed structure & L times less delay elements.

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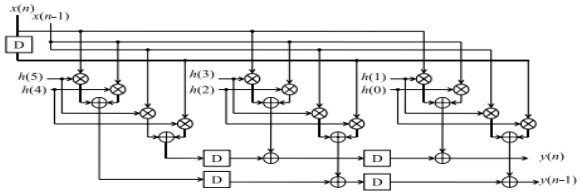

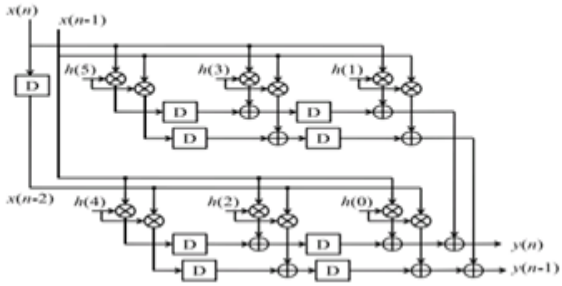

Fig. 4. Merged DFG (DFG-3: transpose form type-I configuration for block FIR structure)

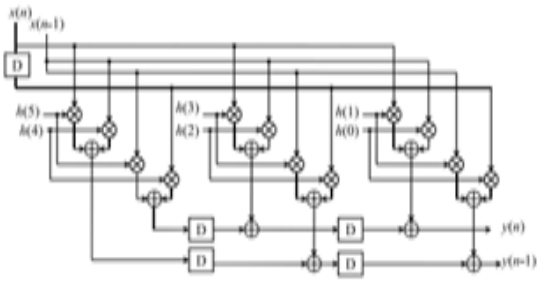

Fig. 5. DFG-4 (retimed DFG-3) transpose form type-II configuration for block FIR structure.

C. Mathematical Formulation of the Transpose Form Block FIR Filter

As discussed in type -2 configuration that FIR filter block produces input samples that process to produce a block output samples. The block filter produces output as

$$yk = Xk \cdot h1704$$

Here h is the weight vector and it is given as

$$h = [h(0), h(1), \ldots, h(N-1)]T$$

At last computation of data flow graph 4 can be expressed in recurrence form as shown below

$$\mathbf{Y}(z) = \mathbf{S}^0(z)[(z^{-1}(\cdots(z^{-1}(z^{-1}\mathbf{c}_{M-1} + \mathbf{c}_{M-2}) + \mathbf{c}_{M-3}) + \cdots) + \mathbf{c}_1) + \mathbf{c}_0] \quad (1$$

III . PROPOSED STRUCTURE

As discussed earlier that there are many applications where the coefficients of FIR filter remain forced but in some applications we use SDR chanalyzer . This chanalyzer has different specifications. Now SDR chanalyzer is implemented on RFIR structure which supports multi standard wireless communication. let us discuss about the proposed structures

A. Proposed Structure for Transpose Form Block FIR Filter for Reconfigurable Applications

The below figure (6) shows the proposed structure for block FIR filters having block size L=4. This proposed structure consists of one coefficient selection unit (CSU), one register unit (RU), M number of inner product units (IPUs), and one pipeline adder unit (PAU)1704. Coming to CSU, it stores the coefficients of all the filters that are used for the reconfigurable application and It is implemented on N ROM LUTs. Due to this the filter coefficients of channel filter are obtained in one clock cycle. Here N is the filter length. This is about CSU now coming to RU it is shown in figure 7(a). At the time of kth cycle RU receives xk and produces L rows of S0k in parallel. These are transmitted to M IPUs of the proposed structure. This M IPUs not only transmits but also receive M short-weight vectors from the CSU. The Fig. 7(b) shows the structure of the (m +1)th IPU. In this It consists of L number of L-point inner-product cells (IPCs). As discussed earlier that result is. Now , the proposed structure receives a block of L inputs and produces a block of L filter added to PAU because to get a block of L filter outputs output, but here a particular duration occurs between each cycle and it is represented as T = TM + TA + TFA log2 L. Here TM is one multiplier delay, TA is one adder delay, and TFA is one full-adder delay1704.

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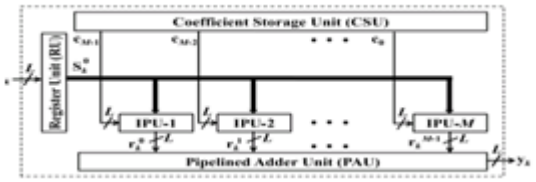

Fig.6. Proposed structure for block FIR filter.

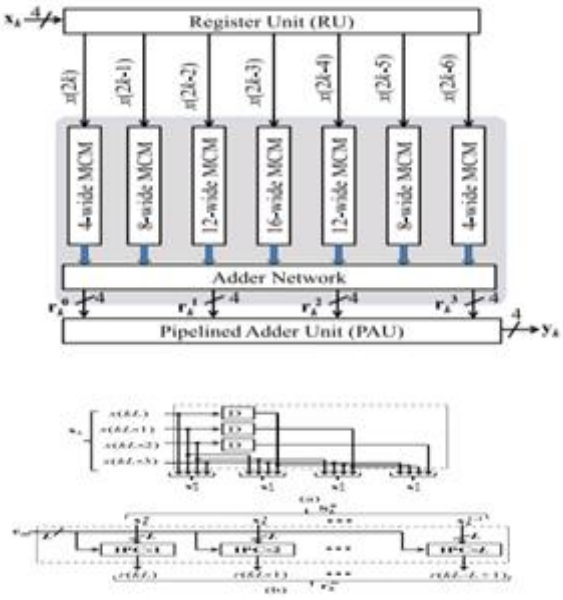

Fig. 7. (a) Internal structure of RU for block size L = 4.
Fig. 7. (b) Structure of (m + 1)th IPU1705

IV. CONCLUSION

At last by using block filters in transpose form configuration it proves that there is a possibility of realization in both fixed and reconfigurable applications. There is a separate block formation in transpose form configuration but for reconfigurable applications There is derived transpose form configuration. To identify MCM blocks of horizontal and vertical sub expression they perform elimination of proposed block FIR filters coefficients. This gives result In performance (.I.e) it has less ADP and EPS compared to the proposed structure result. so from the ASIC , the proposed structure has 42% less ADP and 40% less EPS and for same filter length proposed structure involves 13% less ADP and 12.8% less EPS compared to proposed direct form block FIR structure.

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