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VLSI Architecture of Fm0/Manchester Encoding Using Sols Technique for DSRC Applications

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Abstract:

The dedicated short-range communication (DSRC) is an emerging technique to push the intelligent transportation system into our daily life. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both. The similarity-oriented logic simplification (SOLS) technique is proposed to overcome this limitation. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 × 30.43 μm2.The encoding capability of this project can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works.

Keywords

GMS; GPS; fingerprint; embedded system; vehicle anti-theft protection.

1. Introduction

The dedicated short-range communication (DSRC) is a protocol for one or two way medium range communication especially for intelligent transportation systems. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC enables the message sending and broadcasting among automobiles for safety issues and public information announcement. The safety issues include blind-spot, intersection warning, inter cars distance, and collision-alarm. The automobile-to-roadside focuses on the intelligent transportation service, such as electronic toll collection (ETC) system.

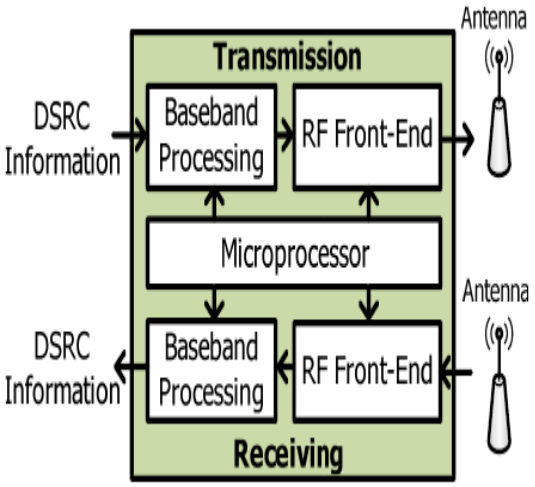


Fig.1.System architecture of DSRC transceiver

The toll collecting is electrically accomplished with the contactless IC-card platform. Moreover, the ETC can be extended to the payment for parking-service, and gas-refueling. Thus, the DSRC system plays an important role in modern automobile industry. The system architecture of DSRC transceiver is shown in Fig.1. The upper and bottom parts are dedicated for transmission and receiving, respectively.

ENCODING

Traditionally, mass communications research has conceptualized the process of communication in terms of a circulation circuit or loop. This model has been criticized for its linearity-sender/message/receiver-for its concentration on the level of message exchange and for the absence of a structured conception of the different moments as a complex structure of relations. But it is also possible (and useful) to think of this process in terms of a structure produced and sustained through the articulation of linked but distinctive moments-production, circulation, distribution/consumption, reproduction. This would be to think of the process as a 'complex structure in dominance', sustained

through the articulation of connected practices, each of which, however, retains its distinctiveness and has its own specific modality, its own forms and conditions of existence. This second approach, homologous to that which forms the skeleton of commodity production offered in Marx's Grundrisse and in Grpital, has the added advantage of bringing out more sharply how a continuous circuit - production-distribution-production - can be sustained through a 'passage of forms'.' It also highlights the specificity of the forms in which the product of the processes appears' in each moment, and thus what distinguishes discursive 'production' from other types of production in our society and in modem media systems.

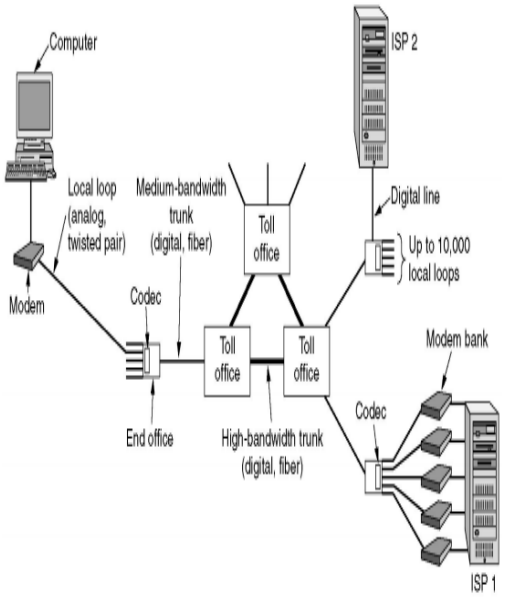


Fig.2. Data encoding

DSRC

The dedicated short-range communication (DSRC) is a protocol for one- or two-way medium range communication especially for intelligent transportation systems. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC enables the messagesending and broadcasting among automobiles for safety issues and public information announcement. The safety issues include blind-spot, intersection warning, intercars distance, and collision-alarm

Sols It is the similarity oriented logic simplification technique used to reduce the number of components in the digital circuit and share the logic of the digital components. This has following types a) Area-Compact Retiming

The FM0 logic for A(t) and the logic for B(t) are the Boolean functions to derive A(t) and B(t), where the X is omitted for a concise representation. For FM0, the state code of each state

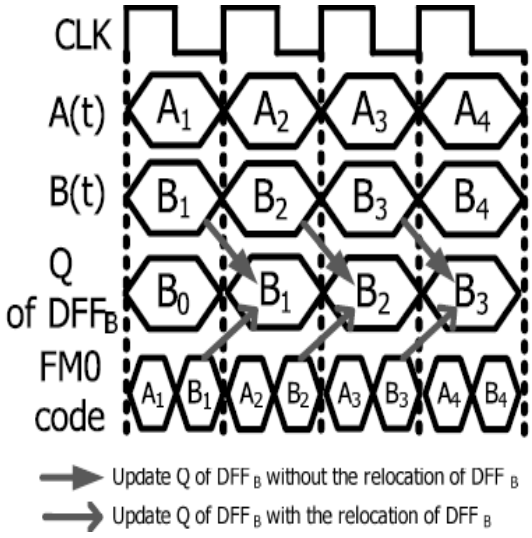


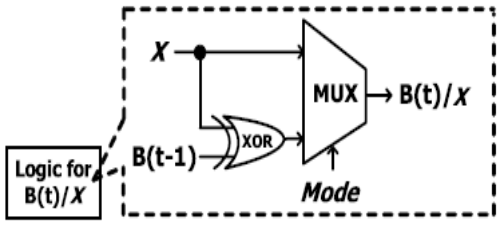
Fig. 3. Timing diagram of area-compact retiming for FM0 encoding.

b) Balance Logic-Operation Sharing As mentioned previously, the Manchester encoding can be derived from X ⊕ CLK, and it is also equivalent to

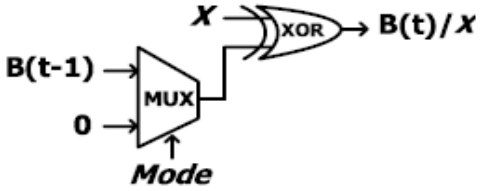
$$X \oplus \mathrm{CLK} = X\,\overline{\mathrm{CLK}} + \overline{X}\,\mathrm{CLK}.$$

This can be realized by the multiplexer, as shown in Fig. 9(a). It is quite similar to the Boolean function of FM0 encoding in (4). By comparing with (4) and (6), the FM0 and Manchester logics have a common point of the multiplexer like logic with the selection of CLK. As shown in Fig. 9(b), the concept of balance logic-operation sharing is to integrate the X into A(t) and X into B(t), respectively. The logic for A(t)/X is shown in Fig. 10. The A(t) can be derived from an inverter of B(t − 1), and X is obtained by an inverter of X. The logic for A(t)/X can share the same inverter, and then a multiplexer is placed before the inverter to switch the operands of B(t − 1) and X. The Mode indicates either FM0 or Manchester encoding is adopted. The similar concept can be also applied to the logic for B(t)/X, as shown in Fig. 11(a). Nevertheless, this architecture exhibits a drawback that the XOR is only dedicated for FM0 encoding, and is not shared with Manchester encoding. Therefore, the HUR of this architecture is certainly limited. The X can be also interpreted as the X ⊕ 0, and thereby the XOR operation can be shared with Manchester and FM0 encodings. As a result, the logic for B(t)/X is shown in Fig. 11(b), where the multiplexer is responsible to switch the operands of B(t−1) and logic-0.

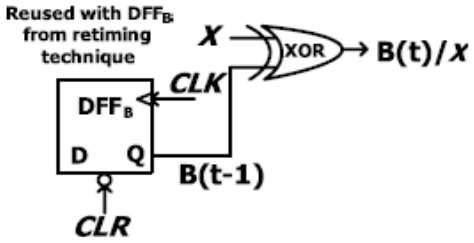
This architecture shares the XOR for both B(t) and X, and thereby increases the HUR. Furthermore, the multiplexer in Fig. 11(b)



(a)



(b)



(c)

Fig. 4. Balance logic-operation sharing of B(t) and X.

(a) Without the XOR sharing. (b) With XOR sharing. (c) Sharing of the reused DFFB from area-compact retiming technique.

c) Timing Analysis The logic functions of SOLS technique can be realized by various logic families. Each logic family optimizes one or more electrical performance, such as area, power, or speed, from circuit topology perspective instead of architecture perspective.

d) Performance Evaluation of the SOLS Technique The evaluation of the SOLS technique is shown in Table V. With SOL's technique, the total components are reduced from seven down to five. Without SOL's technique, the FM0 and Manchester encodings are performed on individual hardware architecture with a poor HUR of 57.14%,

2. Project Design

CODING PRINCIPLES OF FM0 CODE AND MANCHESTER CODE:

In the following discussion, the clock signal and the input data are abbreviated as CLK, and X, respectively. With the above parameters, the coding principles of FM0 and Manchester codes are discussed as follows.

A. FM0 Encoding

For each X, the FM0 code consists of two parts: one for former-half cycle of CLK, A, and the other one for later-half cycle of CLK, B. the coding principle of FM0 is listed as the following three rules.

1) If X is the logic-0, the FM0 code must exhibit a transition between A and B.

2) If X is the logic-1, no transition is allowed between A and B.

3) The transition is allocated among each FM0 code no matter what the X is.

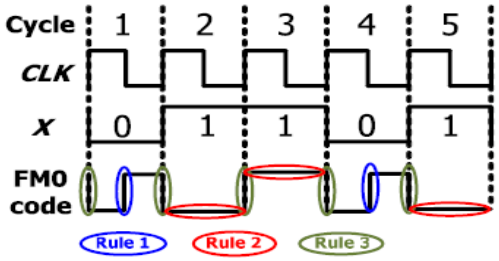


Fig.5. Illustration of FM0 coding example.

B. Manchester Encoding

The Manchester coding example is shown in Fig. 4. The Manchester code is derived fromX ⊕ CLK. The Manchester encoding is realized with a XOR operation for CLK and X. The clock always has a transition within one cycle, and so does the Manchester code no matter what the X is.

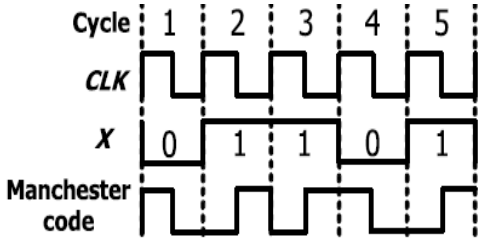
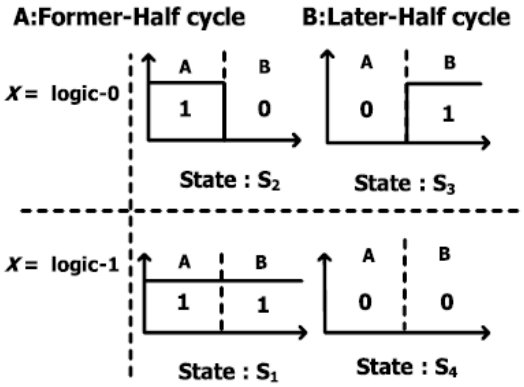


Fig.6. Illustration of Manchester coding example.

I. Limitation Analysis On Hardware Utilization Of Fm0 Encoder And Manchester Encoder

To make an analysis on hardware utilization of FM0 and Manchester encoders, the hardware architectures of both are conducted first. As mentioned earlier, the hardware architecture of Manchester encoding is as simple as a XOR operation. However, the conduction of hardware architecture for FM0 is not as simple as that of Manchester. How to construct the hardware architecture of FM0 encoding should start with the FSM of FM0 first. As shown in Fig. 5(a), the FSM of FM0 code is classified into four states. A state code is individually assigned to each state, and each state code consists of A and B, as shown in Fig. 2. According to the coding principle of FM0, the FSM

of FM0 is shown in Fig. 5(b). Suppose the initial state is S1, and its state code is 11 for A and B, respectively. If the X is logic-0, the state-transition must follow both rules 1 and 3. The only one next-state that can satisfy both rules for



(a)

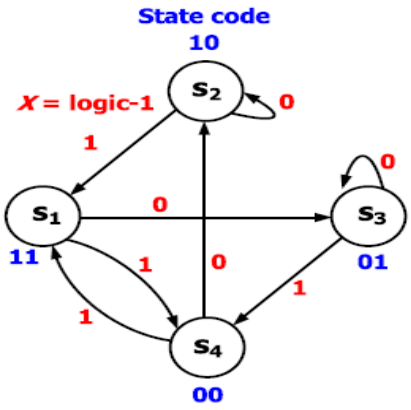


Fig. 7. Illustration of FSM for FM0. (a) States definition. (b) FSM of FM0.

Table 1 Transition Table Of Fm0

Previous-state		Current-state			
		$A(t)$		$B(t)$	
$A(t-1)$	$B(t-1)$	$X=0$	$X=1$	$X=0$	$X=1$
1	1	0	0	1	0
1	0	1	1	0	1
0	1	0	0	1	0
0	0	1	1	0	1

X of logic-0 is S3. If the X is logic-1, the state-transition must follow both rules 2 and 3. The only one next-state that can satisfy both rules for the X of logic-1 is S4. Thus, the state-transition of each state can be completely constructed. The FSM of FM0 can also conduct the transition table of each state, as shown in Table II. A(t) and B(t) represent the discrete-time state code of current-state at time instant t. Their previous-states are denoted as the A(t − 1) and the B(t − 1), respectively. With this transition table, the Boolean functions

HARDWARE ARCHITECTURE OF FM0&MANCHESTER ENCODING

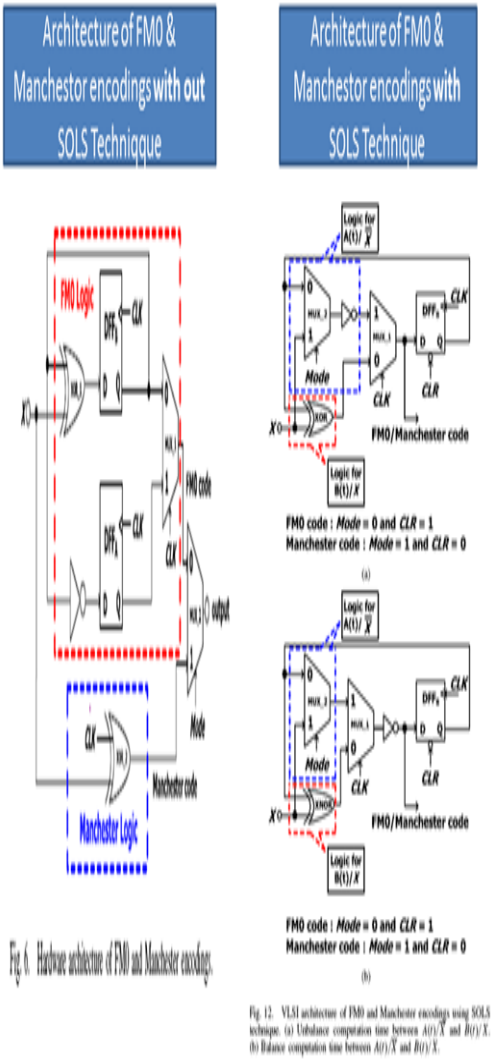


Fig. 8. Hardware architecture of FM0 and Manchester encodings.

3. Results and Discussions

PERFORMANCE EVALUATION OBSERVATIONS					
HARDWARE UTILIZATION RATE(HUR)					
WITHOUT SOLS			WITH SOLS		
Coding Without SOLS	Active Components(transistor count) / Total Components(transistor count)	HUR	Coding With SOLS	Active Components(transistor count) / Total Components(transistor count)	HUR
FMO	6 (86) / 7 (98)	85.71%	FMO	5 (44) / 5 (44)	100%
Manchester	2 (26) / 7 (98)	28.57%	Manchester	5 (44) / 5 (44)	100%
Average	4 (56) / 7 (98)	57.14%	Average	5 (44) / 5 (44)	100%

SIMULATION WINDOWS OF FMO ENCODING

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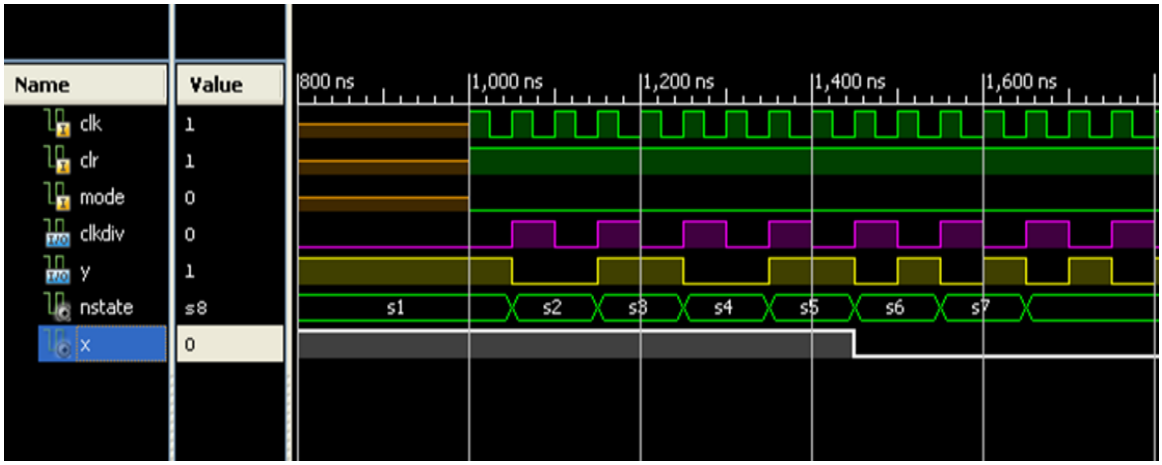

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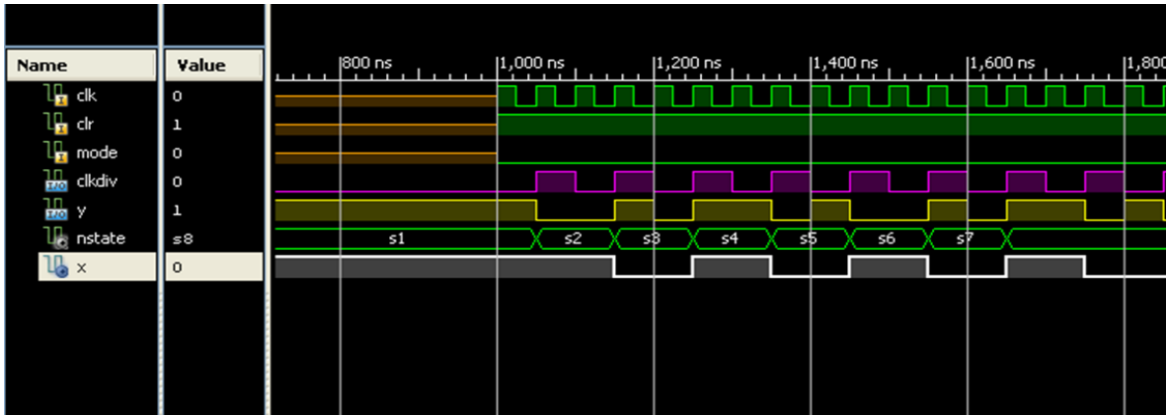

SIMULATION WINDOWS OF MANCHESTER ENCODING

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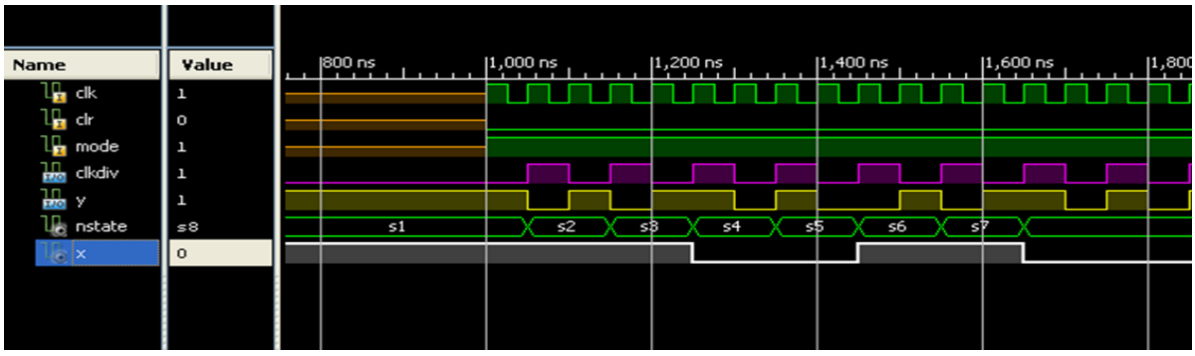

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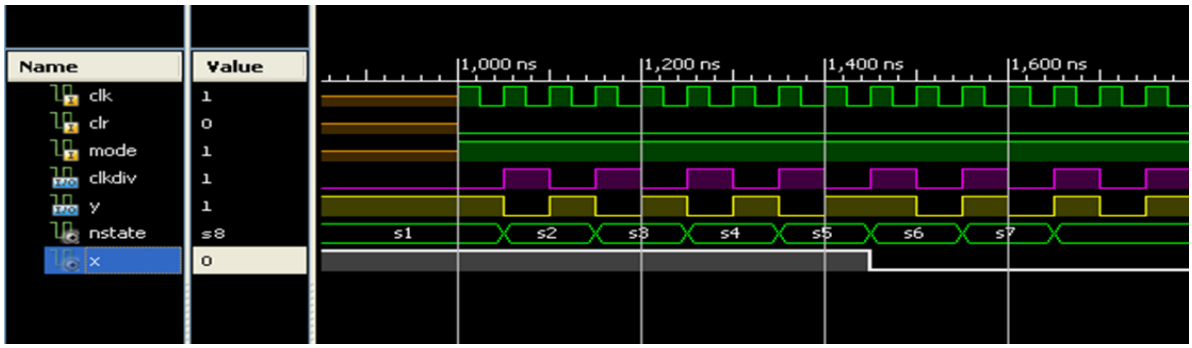

4. Conclusion

The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this project, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This project is realized in TSMC 0.18-µm 1P6MCMOS technology with an outstanding device efficiency. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 × 30.43 µm2. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This project not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works.

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