

A New Nested Neutral Point-Clamped (Nnpc) Converter for Medium-Voltage (Mv) Power Conversion

¹ALIYA ANJUM,²KODEM.CHANDRAMOULI,³DR.M.RAMESH

1.Pg Scholar, Department of EEE, Vaageswari College of Engineering, karimnagar.

2.Associate Professor, Department of EEE, Vaageswari College of Engineering, karimnagar,

3. Professor&Hod, Department Of EEE, Vaageswari College Of Engineering, Karimnagar.

ABSTRACT

In this project presents the NNPC inverter is a newly developed four-level voltage source inverter for medium-voltage applications with properties such as operating over a wide range of voltages (2.4–7.2 kV) without the need for connecting power semiconductor in series and high-quality output voltage. The NNPC topology has two flying capacitors in each leg. In order to ensure that the inverter can operate normally and all switching devices share identical voltage stress, the voltage across each capacitor should be controlled and maintained at one-third of dc bus voltage. The proposed capacitor voltage-balancing method takes advantage of redundancy in phase switching states to control and balance flying capacitor voltages. Simple and effective logic tables are developed for the balancing control

I INTRODUCTION

Nowadays, Multilevel inverters are very popular in medium voltage applications and motor drives due to reduction of harmonics, low voltage stress on switches, low switching frequency, and less switching losses [1]. The multilevel inverters categorized into neutral point clamped (NPC) inverter, flying capacitor (FC) inverter, cascaded Hbridge inverter, and modular multilevel converter [2]–[3]. Several control techniques and modulation strategies including capacitor voltage-balancing methods have been developed in the literature for multilevel inverters [4]. In this paper a new multilevel topology is proposed. i.e, nested neutral point clamped (NNPC) inverter shown in Fig. 1. Fig. 1. Three phase nested neutral-point clamped (NNPC) inverter. This topology is a combination of an FC topology with an NPC topology, which provides four levels in output voltage. In comparison with the fourlevel NPC inverter, the NNPC inverter has less number of diodes, and in

comparison to four-level FC inverter, it has fewer capacitors [6]. All switches in the topology have the same voltage stress equal to one-third of dc-link voltage. The NNPC inverter can operate in a wide range of 2.4–7.2 kV without the need for connecting power devices in series. As can be seen from Fig. 1, the NNPC topology has two FCs in each leg. The voltage across each capacitor should be controlled and balanced at one-third of dc-link voltage ($V_{dc}/3$) to ensure that the inverter can operate normally [6]. In order to mitigate the aforementioned drawbacks, a new capacitor voltage-balancing method for the NNPC inverter is proposed in this paper. In the proposed method, simple logic tables are developed to control the voltages of FCs. The proposed method has the following features: 1) The method is suitable for and can be easily integrated with different pulse width modulation (PWM) schemes such as SPWM and SVM, etc; 2) The method uses simple logic tables, needs very few computations, and is easy to implement. The difference in the topology causes different behavior in capacitor voltages and thus need different voltage-balancing methods. In order to control output voltage and get FC voltage balance, a space vector modulation (SVM) technique is presented in [6] for NNPC

inverter. In this method, a cost function is defined based on the energy stored in capacitors. The cost function needs to be calculated repeatedly for each redundant switching state in every sampling period to find the best switching state to balance FC voltages.

II OPERATION OF THE NNPC INVERTER AND BEHAVIOR ANALYSIS OF THE CAPACITOR VOLTAGES

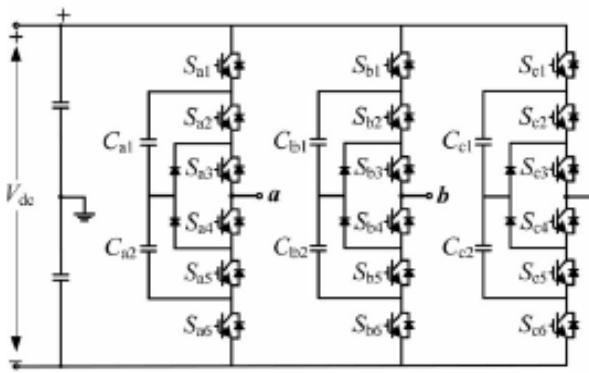
Operation of the NNPC Inverter The three-phase NNPC inverter Each phase of the inverter consists of six switches, two clamping diodes, and two FCs. The voltages of the FCs should be kept at one-third of dc bus voltage ($V_{dc}/3$) to generate four output levels in phase voltage and ensure that all the power switches share the same voltage stress. Table I shows the phase voltage v_k ($k=a, b, c$), output level L_k , as well as the corresponding phase switching state S_k . For each phase, the four distinct output voltages are $-V_{dc}/2$, $-V_{dc}/6$, $V_{dc}/6$, and $V_{dc}/2$, corresponding to the four output levels 0, 1, 2, and 3, respectively.

III PROPOSED METHOD

The proposed method describes capacitor voltage-balancing method takes advantage of redundancy in phase switching

states to control and balance flying capacitor voltages. Simple and effective logic tables are developed for the balancing control. The proposed method is easy to implement and needs very few computations. The method is suitable for and can be easily integrated with different pulse width modulation (PWM) schemes such as SPWM and SVM, etc.;

Block diagram



Three phase nested neutral-point clamped (NNPC) inverter.

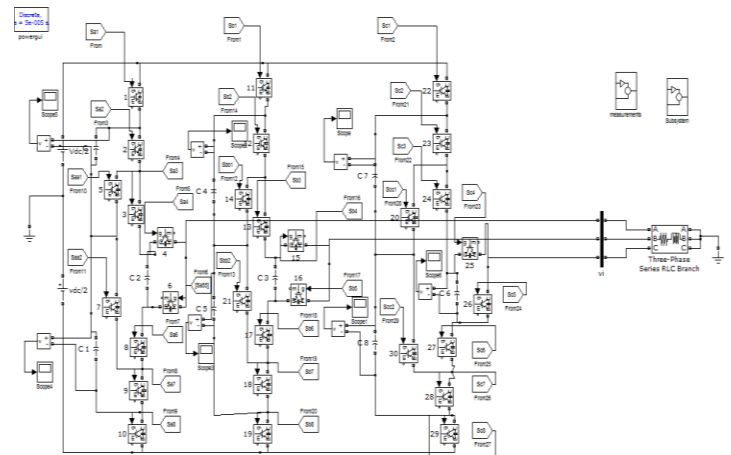
Advantages

- Multi level inverters are very popular in medium voltage power conversion due to low voltage stress on switches,
- Better harmonic performance,
- Low switching frequency,
- And less switching losses.

Applications

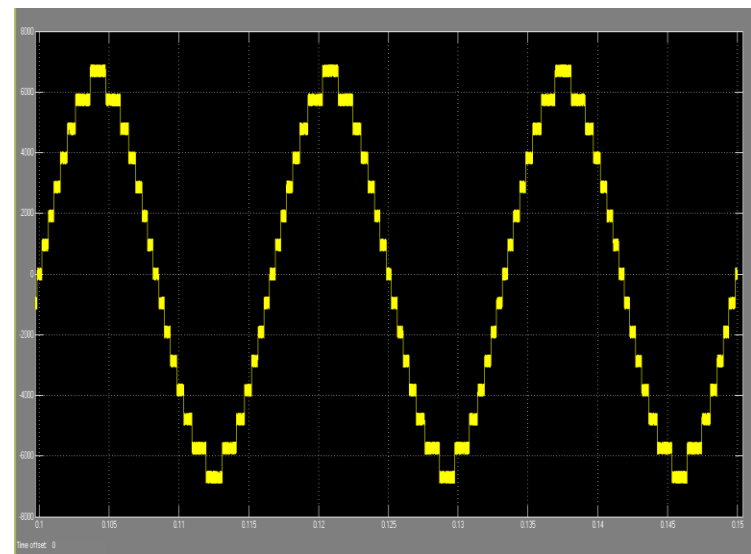
- A wide range of voltages (2.4–7.2 kV) without the need for connecting power semiconductor in series and high-quality output voltage.
- Multilevel inverters, drives.

IV RESULTS:

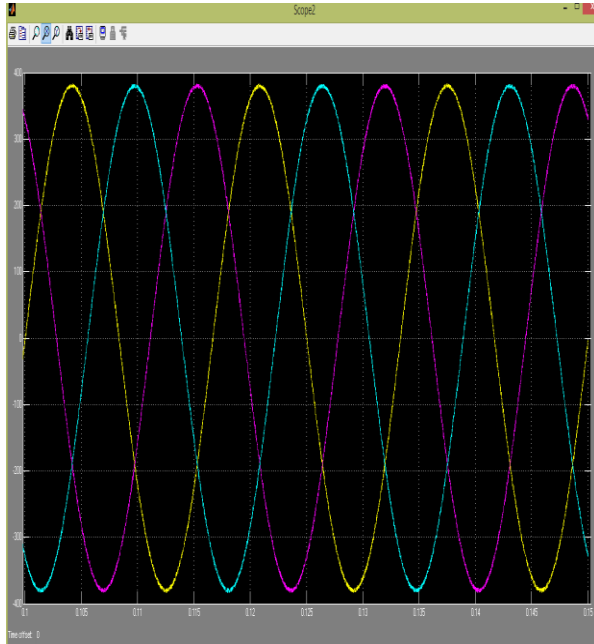


. Steady-state simulation with m=0.95

output Voltage

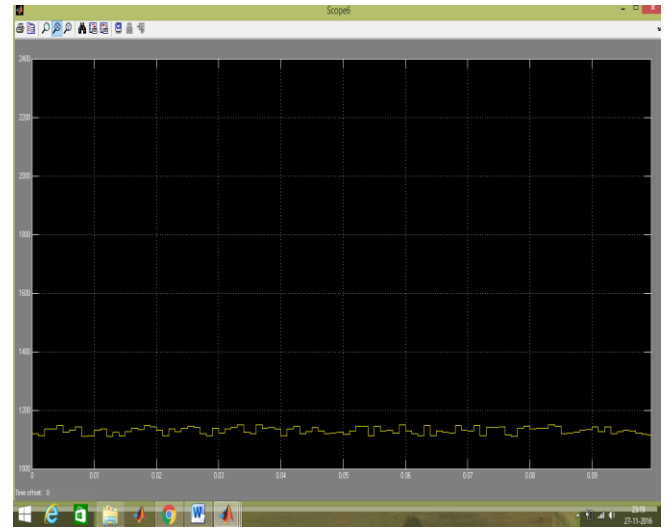


Output currents

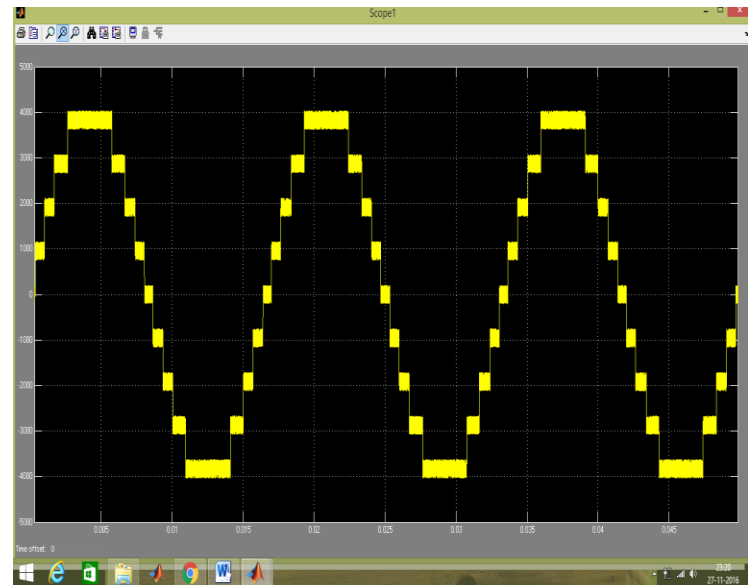
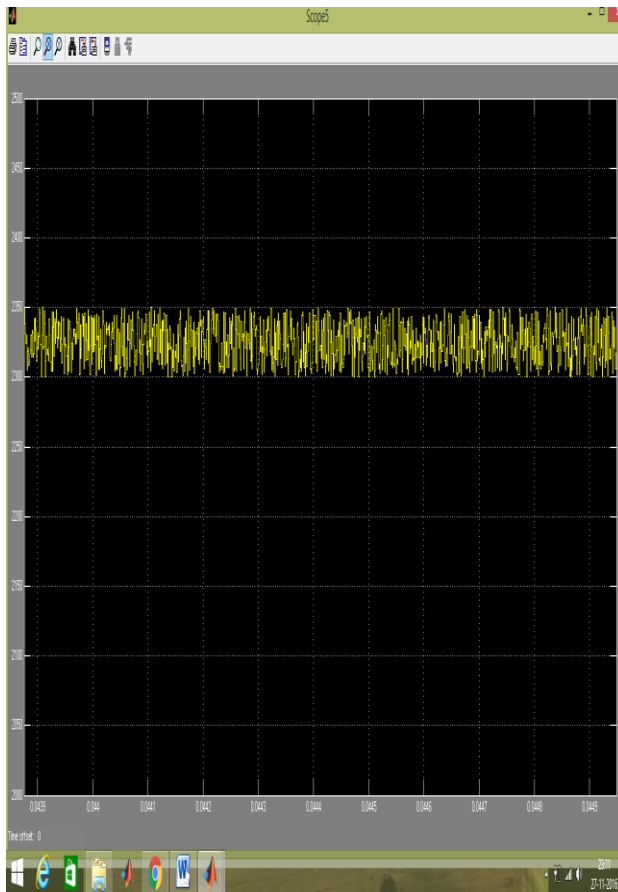


flying capacitor voltage

c1, c2



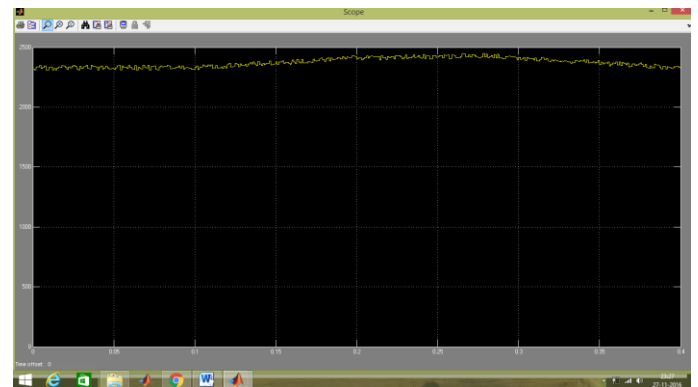
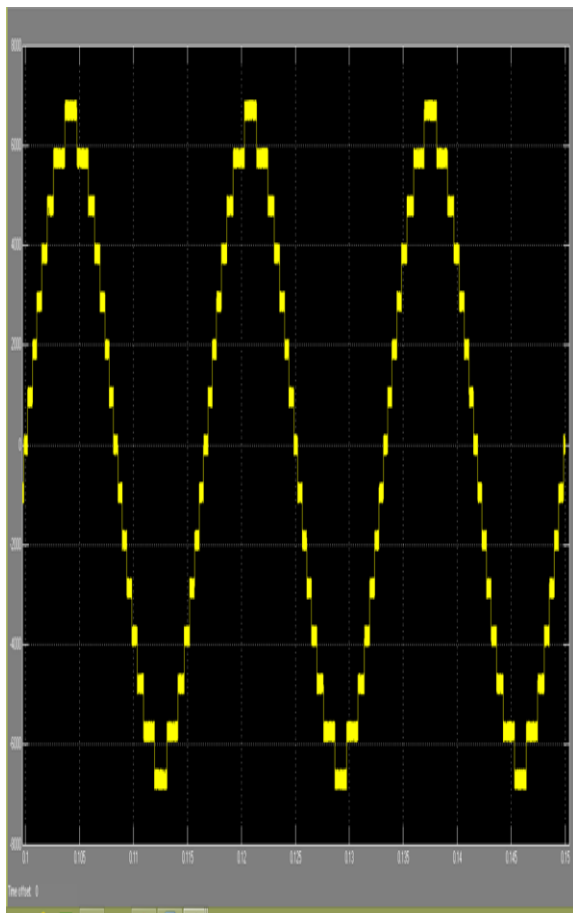
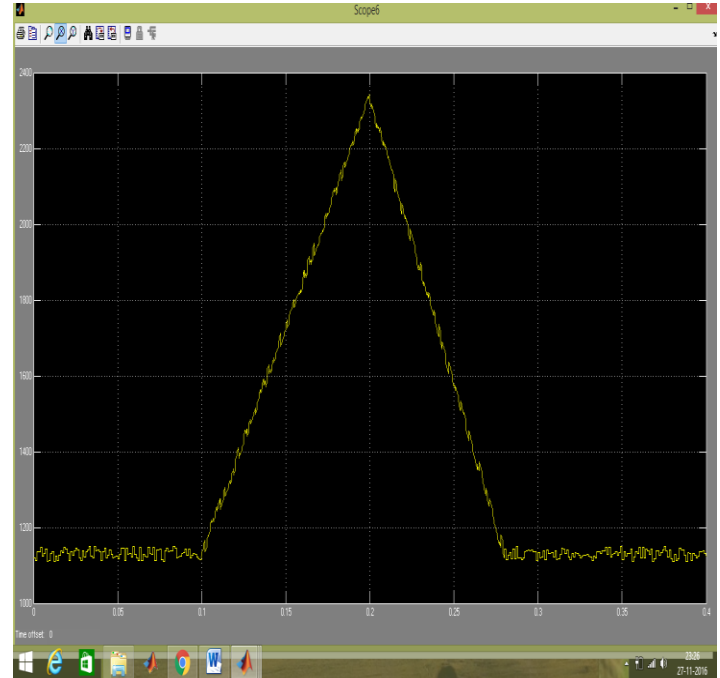
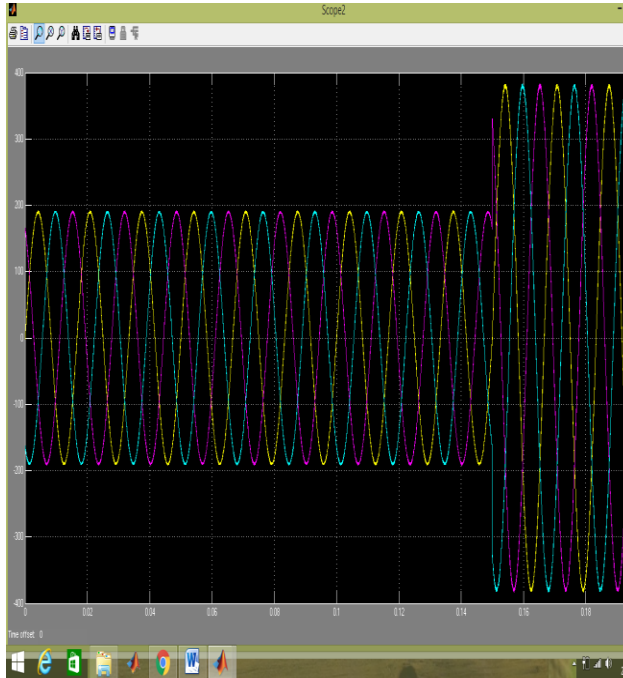
Steady-state simulation with $m=0.60$



B. Transient-State Analysis

Load C hanging

Output currents



V CONCLUSION

In this paper, proposes a capacitor voltagebalancing method for a four-level NNPC inverter. At different PWM schemes the proposed method is easy to integrated. The proposed method takes advantage of redundancy in phase switching states to control and balance the FC voltages. For the control of capacitor balancing simple and effective logic tables are developed. The

method is easy to implement and needs very few computations. The limitation of the NNPC inverter in terms of the voltage balancing and capacitor size is also investigated. The effectiveness and feasibility of the proposed method is determined by using the simulation results and also analyze the proposed method.

REFERENCES

- [1] B. Wu, *High-Power Converters and AC Drives*. New York, NY, USA: Wiley/IEEE Press, 2006, ch. 1.
- [2] N. Mittal, B. Singh, S. P. Singh, R. Dixit, and D. Kumar, "Multilevel inverters: A literature survey on topologies and control strategies," in *Proc. 2nd Int. Conf. Power, Control Embedded Syst.*, 2012, pp. 1– 11.
- [3] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002. [4] R. Stala, "A natural dc-link voltage balancing of diode-clamped inverters in parallel systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5008–5018, Nov. 2013.
- [5] J. Mei, K. Shen, B. Xiao, L. M. Tolbert, and J. Zheng, "A new selective loop bias mapping phase disposition PWM with dynamic voltage balance capability for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 798–807, Feb. 2014.
- [6] M. Narimani, B. Wu, Z. Cheng, and N. Zargari, "A new nested neutral point clamped (NNPC) converter for medium-voltage (MV) power conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 5259–5270, Dec. 2014.
- [7] A. Choudhury, P. Pillay, and S. S. Williamson, "DC-link voltage balancing for a three-level electric vehicle traction inverter using an innovative switching sequence control scheme," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 2, pp. 296–307, Jun. 2014.
- [8] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM With dc-link capacitor voltage balancing control for diode-clamped multilevel converter based
- [9] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, "Voltage balancing control of diodeclamped multilevel converters with passive frontends," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1751–1758, Jul. 2008..
- [10] S. Busquets-Monge, R. Maheshwari, and S. Munk-Nielsen, "Overmodulation of

n-Level three-leg dc-ac diode-clamped converters with comprehensive capacitor voltage balance,"IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1872–1883, May 2013.

[11] A. H. Bhat and N. Langer, "Capacitor voltage balancing of three-phase neutral-point-clamped rectifier using modified reference vector, "IEEE Trans. Power Electron., vol. 29, no. 2, pp. 561–568, Feb. 2014

AUTHOR'S PROFILE:



ALIYA ANJUM,

Pg Scholar, Department of EEE, Vaageswari College of Engineering, karimnagar



ODEM.CHANDRAMOULI.

Assoc.Prof., Department of EEE, Vaageswari College of Engineering, karimnagar

Dr. M. Ramesh was born in Guntur District, Andhra Pradesh, on 07-06-1977. I completed my B.Tech. (EEE) from Viswanadtha Institute of Technology and Management affiliated Jawaharlal Nehru

Technological University, Hyderabad in 2002, M. Tech.(Advanced Power Systems) from Jawaharlal Nehru Technological University, Kakinada,



Andhra Pradesh in 2005 and completed Ph.D.(Application of Artificial Intelligent

Techniques for Enhancement of Stability in HVDC Transmission System) from Jawaharlal Nehru Technological University College of Engineering, Ananthapuram in 2017. I have one year of Industrial experience and 15 years of teaching experience and presently working as a Professor and HOD, EEE Dept, Vaageswari College of Engineering, karimnagar Dist. I published 30 International Journals to my credit. I published 10 International and National papers in various conferences held at India and also abroad. My research interests are AI Techniques, Power Systems & FACTS. I have Member in IEEE, Life Member of Indian Society of Technical Education (M.I.S.T.E), Life Member International Association of Computer Science and Information Technology, Life Member of International Association of Engineers, Member of Engineering Council of India (MECI)