Low Power Ripple Carry Adder Design Using MTCMOS Technique

S. Veereshwara Rao[1] & K. Padmaja Devi[2]

1 (PG Scholar, Dept. of ECE, TKR College of Engineering and Technology, Hyderabad, India)

2(Faculty, Dept. of ECE, TKR College of Engineering and Technology, Hyderabad, India)

Email: vikramfriends7@gmail.com

ABSTRACT

Adders form an almost obligatory component of every contemporary integrated circuit. For the design and analysis of complex arithmetic circuits low power performance measuring parameters like leakage current and active power are plays important role in that. In this paper standby power and the Active power are considerably reduced by the use of sleep transistor in full adder design and 8 bit Ripple carry adder. Size of the sleep transistor is determined by transistor resizing approach. Here also describes header or footer switch selection. 8 bit Ripple carry adder is implemented using 1 bit adder as reference. The simulation shows that, the 1 bit and 8 bit Ripple carry adders are efficient in terms of standby leakage power and active power. Simulations have been performed using H-Spice 90nm and 65nm CMOS technology.

Key words-

sleep transistor; Leakage power; adder cell; Active power

1. INTRODUCTION

Leakage power has been increasing exponentially with the technology scaling. Any computational circuit is incomplete without the use of an adder. Addition is one of the primary operations in arithmetic circuits [1], [2].These adder cells commonly aimed to reduce power consumption. These studies have also investigated different approaches realizing adders using CMOS technology [3], [4]. The designer's concern for the level of leakage current is mainly aimed at minimizing power dissipation. Leakage power reduction becomes critical in low-power applications such as cell phone and handheld terminals.

For portable electronic devices this equates to maximizing battery life. For example, mobile phones need to be powered for extended periods (known as standby mode, during which the phone is able to receive an incoming call), but are fully active for much shorter periods (known as talk or active mode, while making a call). When a mobile phone is in standby mode, certain portions of the circuitry are shut down. Even though de-activated, these circuits have some leakage current flowing through them.

Even if the leakage current is much smaller than the normal operating current of the circuit, it depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time. As a result, the leakage current has a disproportional effect on total battery life. Each new technology generations results nearly a 30xincrease in gate leakage [7], [8].

There are several techniques to reduce leakage power. MTCMOS technique is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground) [8]. This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in

leakage at a minimal impact on performance [9], [10].

2. MTCMOS TECHNIQUE

2.1 SLEEP TRANSISTOR IMPLEMENTATION

A sleep transistor is referred to either a PMOS or NMOS high V_{th} transistor that connects permanent power supply to circuit power supply which is commonly called "virtual power supply".

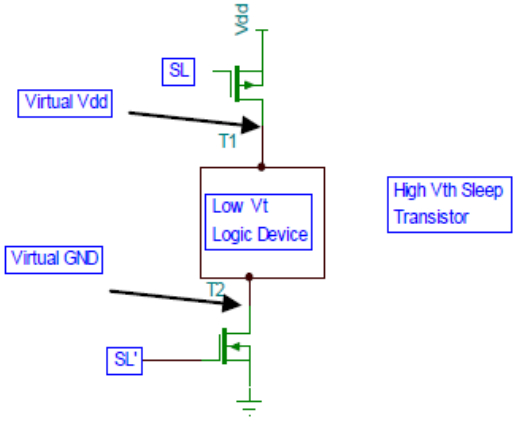

Fig 1 Sleep Transistor Connection

The sleep transistor is controlled by a power management unit to switch on and off power supply to the circuit. The PMOS sleep transistor is used to switch VDD supply and hence is named "header switch". The NMOS sleep transistor controls VSS supply and hence is called "footer switch". In this we can use either header or footer switch is only due to decrease the area of device.

2.2 HEADER SWITCH

The header switch is implemented by PMOS transistors to control V_{dd} supply. Header switches turn off VDD and keep VSS on.

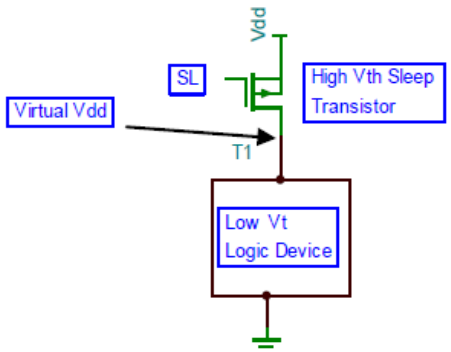

Fig 2 Header Sleep Transistor

The disadvantage of the header switch is that PMOS has lower drive current than NMOS of a same size, though difference is reduced by strained silicon technology. As a result, a header switch implementation usually consumes more area than a footer switch implementation.

2.3 FOOTER SWITCH

The footer switch is implemented by NMOS transistor to control VSS supply. The advantage of footer switch is the high drive and hence smaller area.

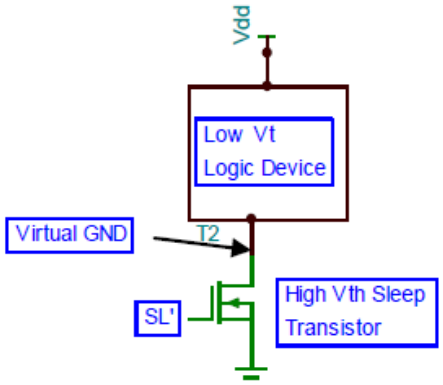

Fig 3 Footer Sleep Transistor

3. FULL ADDER BLOCK DIAGRAM IMPLEMENTATION

Now a day's power dissipation has became an important concern in portable

electronic devices.The full adder will be designed with the 28 number of transistors. So that here we are giving a, b and C_{in} as inputs and we will get the sum and carry as the outputs. For that to get the sum and carry as outputs, we need logical XOR and logical AND and logical OR operations. In the below design at left side we have the carry output by doing the AND and OR operations. And at right side by the XOR operations we will get the sum as output. And here we know that If two NMOS transistors are in series or if two PMOS transistors are in parallel then that is logical AND operation. And if two NMOS transistors are in parallel or If two PMOS transistors are in parallel then that is logical OR operation.Static logic style gives robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS and Pass-transistor logic can reduce the number of transistors required to implement a given logic function. But those suffer from static power dissipation. Implementing Multiplexers and XOR based circuits are advantageous in pass transistor logic [4].

On the other hand, dynamic logic implementation of complex function requires a small silicon area but charge leakage and charge refreshing are required which reduces the frequency of operation. In general, none of the mentioned styles can compete with CMOS style in robustness and stability [4]. The conventional CMOS 28 transistor adder [7], as shown in Figure 4, is considered as Base case throughout this paper. All comparisons are done with Base case. Transistor sizes are specified as a ratio of Width/Length (W/L). It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is 2 for an inverter. This ratio proves inefficient in when simulated below 90nm process. Hence, the gate resized adder circuits are used as shown in Figure 4, 5, 6. Further, power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. The smallest transistor considered for 90nm technology has a width of 120nm and a length of 100nm and for 65nm technology has a width of 78nm and a length of 65nm which gives W/L ratio of 1.2. The W/L ratio of NMOS is fixed at 1.2 and W/L of PMOS is 3.8 which is 3.1 times that of NMOS in Design1 (Figure 5).

The sizing of each block is based on the following assumption. These sizing will reduce the standby leakage current greatly because sub-threshold current is directly proportional to the width/length ratio of transistor. On the other hand, these reduced sizes reduce area occupied by the circuit. This will reduce the silicon chip area in turn reduced in cost.

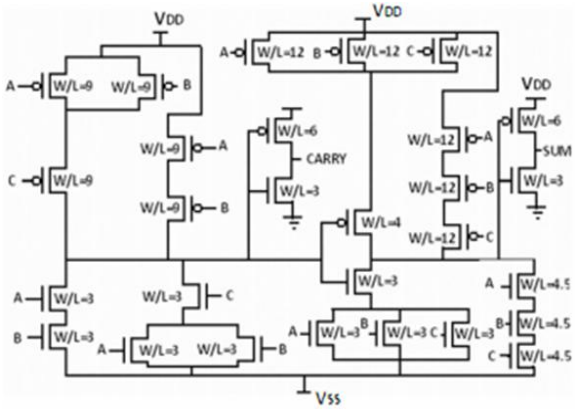

Fig 4 Conventional CMOS full adder

Modified adder circuit of Design 2 shown in figure 6, the W/L ratio of PMOS is 1.5 times that of W/L ratio of NMOS and each block has been treated as an equivalent inverter. The goal of this design is to reduce the standby leakage power.

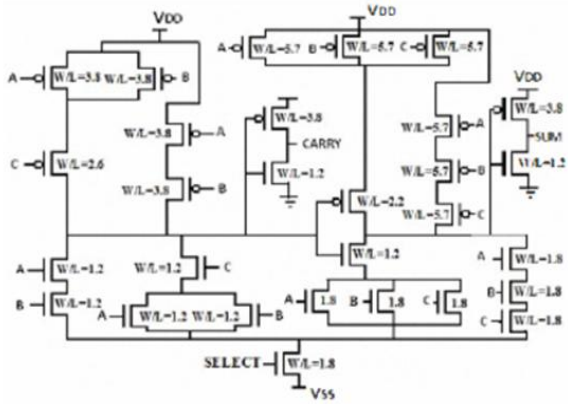

Fig 5 Full adder (Design 1) with Sleep transis

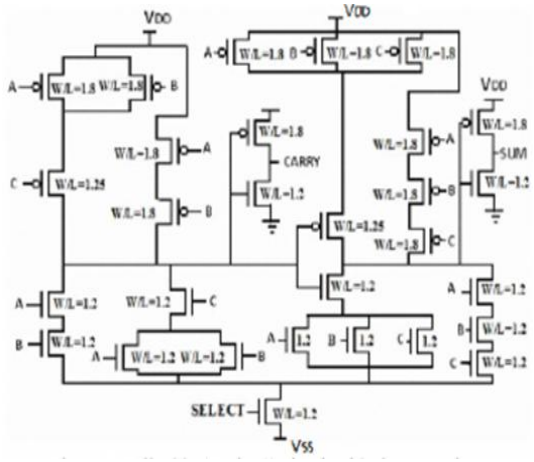

Fig 6 Full adder (Design 2) with Sleep transistor

4. POWER ANALYSIS AND SIMULATION RESULTS

We have performed simulations using H-Spice simulator and technology being employed in 90nm and 65nm with supply voltage of 1.2v for power analysis of 1 bit and 8 bit adders. Different power consumptions are

Dynamic (or switching) power consumption occurs when signals which go through the CMOS circuits change their logic state charging and discharging of output node capacitor.Leakage power consumption is the power consumed by the sub threshold currents and by reverse biased diodes in a CMOS transistor.Short circuit power consumption occurs during switching of both NMOS and PMOS transistors in the circuit and they conduct simultaneously for a short amount of time.

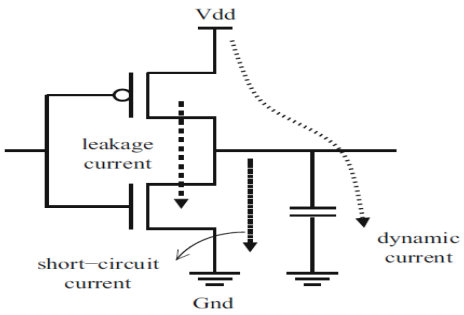

Fig 7 Different Powers

The simulation results of the full adder with sleep transistor and without Sleep transistor are observe in below two diagrams. In without sleep transistor result we can clearly understand that the output wave forms (Sum and Carry) are available throughout. In with Sleep transistor results we can clearly understand that the output wave forms (Sum and Carry) are available only when the sleep transistor is in High.

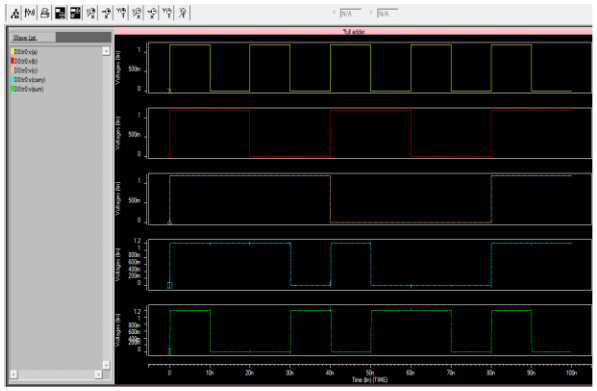

Fig 8simulation result of adder without Sleep Transistor

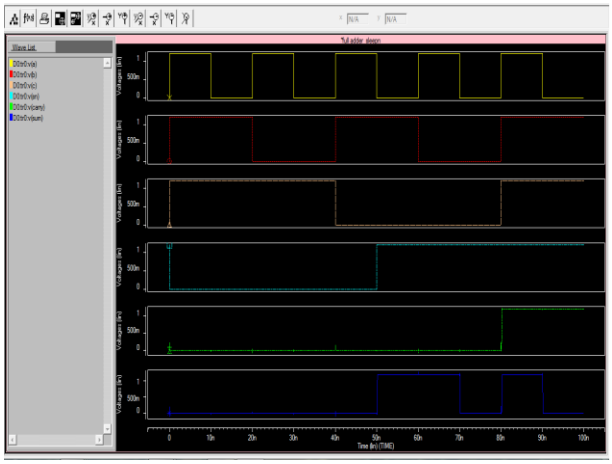

Fig 9 simulation result of adder with Sleep Transistor

4.1 ACTIVE POWER

Power dissipated by circuit when the circuit is in active state is termed as Active power. Input vectors are fed into the circuit and the average power dissipation is measured. Here, considered simulation time for active power is

80ns. Almost all of the input combinations are considered for simulation. Same input vector combinations have been given to the all three designs Base case, Design 1 and Design 2, and comparison has been made for the same in both 90nm and 65nm technology. Table 1 and 2 shows comparison of different adders for active power in mW (micro watts).

Table 1. Comparison of Active power of three designs in 90nm

	90nm conv	90nm Design1	90nm Design2
000	2.035	0.912	0.505
001	2.654	0.091	0.062
010	2.876	0.798	0.429
011	1.604	0.0436	0.0247
100	0.5274	0.241	0.113
101	0.4402	0.016	0.011
110	4.413	0.134	0.055
111	5.4301	0.416	0.185

Table 2: Comparison of Active power of three designs in 65nm

	65nm conv	65nm Design1	65nm Design2
000	1.658	0.726	0.428
001	2.198	0.429	0.188
010	2.431	0.719	0.391
011	1.351	0.251	0.068
100	0.415	0.186	0.088
101	0.329	0.161	0.079
110	3.921	0.101	0.046
111	4.239	0.285	0.131

4.2 STANDBY POWER

Standby leakage power is measured when the circuit is in standby mode. Sleep transistor is connected to pull down network of 1 bit full adder circuit. Sleep transistor is off asserting an input 0V. The size of sleep transistor in Design 1 and Design 2 is reduced due to resizing of the adder cells in proposed circuit. Standby leakage power is measured by giving different input combinations to the circuit. Standby leakage is greatly reduced in both Design 1 and Design 2 and for both 90nm and 65nm. as shown Table 3 and 4 shows comparison of different adders for standby power in nW (nano watts).

Table 3: Comparison of Standby power of three designs in 90nm

	90nm conv	90nm Design1	90nm Design2
000	0.2705	0.1489	0.088
001	0.48054	0.1555	0.095
010	0.4733	0.1525	0.097
011	0.4564	0.1513	0.096
100	0.4659	0.1533	0.099
101	0.4341	0.1479	0.097
110	0.4237	0.1571	0.012
111	0.57271	0.1718	0.082

Table 4: Comparison of Standby power of three designs in 65nm

	65nm conv	65nm Design1	65nm Design2
000	5.401	2.958	1.664
001	9.889	3.219	1.921
010	9.863	3.211	2.028
011	9.643	3.261	2.065
100	9.552	3.104	1.956
101	9.055	3.07	1.965
110	8.604	3.131	1.98
111	11.06	3.342	1.56

4.3 8 BIT RIPPLE CARRY ADDER ACTIVE AND STANDBY POWER

Full adder cells shown in Figure 4, 5 and 6 are used to design 8 bit ripple carry adders in all three designs- Conventional, Design 1 and Design 2, for both 90nm and 65nm technology, are constructed as shown in Figure 8. The active power and standby power are calculated in mW (micro watts) and nw (nano watts) respectively in both 90nm and 65nm are shown in Tables 5 to 8.

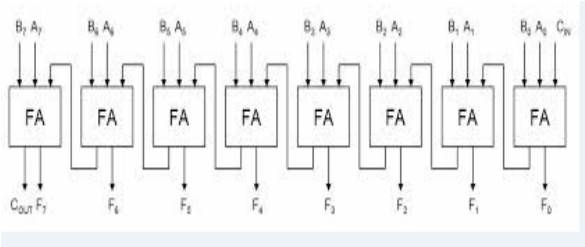

Fig 8 8-bit Ripple Carry Adder

Table 5: Comparison of Active Power of 8 bit RCA for three designs in 90nm

	90nm conv	90nm Design1	90nm Design2
combination 1	8.42	2.16	0.18
combination 2	3.29	0.74	0.11
combination 3	30.39	8.1	0.92
combination 4	54.43	12.27	2.76

Table 6: Comparison of Active Power of 8 bit RCA for three designs in 65nm

	65nm conv	65nm Design1	65nm Design2
combination 1	6.68	2.99	1.78
combination 2	2.84	1.16	0.61
combination 3	24.5	10.89	6.68
combination 4	44.53	20.69	10.58

Table 7: Comparison of Standby Power of 8 bit RCA for three designs in 90nm

	90nm conv	90nm Design1	90nm Design2
combination 1	4.13	1.33	0.68
combination 2	4.34	1.34	0.69
combination 3	4.46	1.35	0.67
combination 4	4.58	1.37	0.65

Table 8: Comparison of Standby Power of 8 bit RCA for three designs in 65nm

	65nm conv	65nm Design1	65nm Design2
combination 1	80.38	26.14	13
combination 2	84.87	26.4	13.26
combination 3	87.08	26.65	12.98
combination 4	88.5	26.73	12.48

5. CONCLUSION

In this paper Active power and Leakage Power are analyzed for Conventional and Modified (Sleep transistor connected) 1-bit Adder circuits, in 90nm and 65nm technology. 8-bit Ripple carry adder is designed based on 1-bit full adder and the adders are analyzed for active and standby power in both 90nm and 65nm technology. Standby power or leakage power of Design1 and Design2 is reduced by almost 50% to 60% than the conventional design respectively. Active power dissipation is reduced by almost 45% and 60% by using Design1 and Design2 respectively.

6. REFERENCES

[I] Radu Ziatanovici, Sean Kao, Borivoje Nikolic, "Energy-Delay of Optimization 64-Bit Carry- Lookahead Adders With a 240ps 90nm CMOS Design Example," IEEE J Solid State circuits, vo1.44, no. 2, pp. 569-583, Feb. 2009.

[2] K.Navi, O. Kavehei, M. Rouholamini, A. Sahaf, S. Mehrabi, N.Dadkhai, "Low-Power and High-Performance I-bit CMOS Full Adder Cell," Journal o/Computers, Academy Press, vol. 3, no. 2, Feb. 2008.

[3] Rabaey J.M.,A.Chandrakasan, B.Nikolic,Digital Integrated Circuits,A Design Perspective, 2nd Prentice Hall, Englewood Clifs, NJ, 2002.

[4] Pren R. Zimmermann, W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid- State Circuits, vol. 32, pp. 1079- 1090, July 1997.

[5] S.G.Narendra and A. Chandrakasan, Leakage in Nanometer CMOS Technologies. New York: Springer-verlag, 2006.

[6] K.Berstein et aI., "Design and CAD challenges in sub-90nm CMOS technologies," in Proc. int. conf comput. Aided Des., 2003, pp. 129- 136.

[7] N.West. K.Eshragian, Principles of CMOS VLSI Design: A systems Perspective, Addison-wesley, 1993.

[8] Ku He, Rong Luo, Yu Wang, "A Power Gating Scheme for Ground Bounce Reduction During Mode Transition, " in ICCD07, pp. 388-394, 2007.

[9] M. V D. L.Varaprasad, Rohit Bapna, Manisha Pattanaik, "Performance Analysis of Low leakage I-bit Nano-CMOS Based Full Adder Cells for Mobile Applications," Proceedings International Conference on VLSI Design & Communication Systems, pp.233-238, January 2010.

[10] M. V D. L. Varaprasad, Fazal Rahim Khan, Manisha Pattanaik, "Ground Bounce Noise Reduction of Low leakage I-bit Nano-CMOS based Full Adder Cells for Mobile Applications", 2010 interational conference on Electronic devices, Systems and applications (ICEDSA2010), pp.31-36.

7. AUTHOR BIOGRAPHY

S.Veereshwara Rao

S. Veereshwara Rao was born in kodad, India, in 1991. He received the B.Tech Degree in Electronics and Communication Engineering From JNTU, Hyderabad in 2012. He is pursuing M.Tech VLSI Design at TKR College of Enginnering and Technology, Hyderabad, India.

Email: vikramfriends7@gmail.com

K. Padmaja Devi received the B.Tech degree from JNTUA, Ananthapur, India in 1999, the M.Tech degree with specialization DSCE from JNTUH, Hyderabad, India. She is pursuing Ph.D from Rayalaseema University, Karnool, India. She has published 6 national and International papers. Currently, she is an Associate Proffessor in the Electronics and Communication Engineering Department, TKR College of Engineering Technology, Hyderabad, India. She is member of ISTE and IETE, India.

Email: ved_paddu@yahoo.co.in